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Gbps wireless radio and Gbps wireless optical communications

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Editor(s):	**Jorge GARCIA-MARQUEZ (Oledcomm)**
Author(s):	**Guillaume Vercasson, Rodolphe Legouable, Jean Dion (B<>com), Brzozowski Marcin, Sark Vladica (IHP), Camilo Valencia, Jorge Garcia-Marquez, Huetzin Perez-Olivas (Oledcomm), Olivier Bouchet (Orange), Mir Ghoraishi (pureLiFi), Ravinder Singh, Dominic O'Brien, Grahame Faulkner (University of Oxford), Rafael Pérez, Víctor Guerra, José Rabadan (Universidad de las Palmas)**
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Abstract
This deliverable will focus on the following items for research in data transmission technology focusing virtual reality use-case:

- Specifications and performance evaluation of a Gbps radio system (radio analog/digital and baseband processing),
- Specifications and performance evaluation of a Gbps optical wireless communication (OWC) system (optical/digital and baseband processing),
- Common Gbps radio and OWC modem architecture definition with control selection.
- Global architecture for V1 demonstrator,
- Scenario to be implemented (video format, SoTA about VR equipment including protocols)
- Optical transmission (throughput objectives, technology choices, simulations performance, link budget, latency estimation, HW targeted board, potential risks, dataflow interconnection)
- Radio transmission (throughput objectives, technology choices, simulations performance, link budget, latency estimation, HW targeted board, potential risks, dataflow interconnection)
- Common optical/radio components (potential common architecture)
- MAC layer issues (Protocol description, implementation, latency constraints, potential risks, dataflow interconnection)
- Video processing
- Conclusion/perspectives (synthesis and global architecture view)

Keyword list
Virtual Reality, High Quality / Low Latency, Wireless, OWC, radio transmission, Mac layer, HW implementation

Executive Summary

This task focuses on virtual reality use-case data transmission permitting to:
a) Specify and evaluate the performance of a Gbps radio system that includes analog/digital radio and baseband processing,
b) Specify and evaluate the performance of a Gbps Optical Wireless Communications (OWC) system, this is, the optical/digital and baseband processing,
c) Define a common Gbps radio and OWC architecture with control selection.
Inputs from WP2 permit in WP3 to design the wireless radio and OWC physical layer system. Here, the architecture for radio and OWC system includes now all the elements of the transmission chain such as the digital baseband processing (coding, modulation, link adaptation, framing, detection, estimation) and the radio and optical front-end stages (antenna design, impairments, ADC/DAC, amplification, filtering). For the WORTECS proof-of-concept PoC, positioning and tracking is also described. The system's architecture consider the results on modelling propagation channel, radio high and very high frequencies and AWC transmissions and asymmetry in data rates for uplink and downlink.
A decision matrix that lists all the potential components has been included which will permit to select the main elements that will be implemented in the final PoC. For the building of such a matrix, complexity evaluation and implementation feasibility have been taken into account.

Impact on the other Work-packages
Input from WP2
The design of wireless radio and OWC physical layer is based on inputs from WP2.

Output towards WP4
A decision matrix that lists all the potential components has been included which will permit to select the main elements that will be implemented in work package WP4.
Selection and specifications of radio and optics system will be provided to WP4. These components takes into account complexity evaluation and HW implementation feasibility as well as platform capabilities and the amount of resources dedicated to the HW implementation. The final specifications will be defined through an iterative process between WP3 and WP4.

List of Authors

First name	Last name	Beneficiary	Email address
Guillaume	Vercasson	b<>com	guillaume.vercasson@b-com.com
Rodolphe	Legouable	b<>com	Rodolphe.legouable@b-com.com
Jean	Dion	b<>com	jean.dion@b-com.com
Marcin	Brzozowski	IHP	brzozowski@ihp-microelectronics.com
Vladica	Sark	IHP	sark@ihp-microelectronics.com
Mir	Ghoraishi	pureLiFi	mir.ghoraishi@purelifi.com
Jorge	García-Márquez	OLD	jorge.garcia@oledcomm.com
Camilo	Valencia	OLD	camilo.valencia@oledcomm.com
Huetzin	Perez	OLD	huetzin.perez@oledcomm.com
Olivier	Bouchet	ORANGE	olivier.bouchet@orange.com
Ravinder	Singh	UOXF	ravinder.singh@eng.ox.ac.uk
Grahame	Faulkner	UOXF	grahame.faulkner@eng.ox.ac.uk
Dominic	O'Brien	UOXF	dominic.obrien@eng.ox.ac.uk
Rafael	Pérez Jiménez	ULPGC	rperez@dsc.ulpgc.es
José	Rabadán	ULPGC	jose.rabadan@ulpgc.es
Víctor	Guerra Yáñez	ULPGC	victor.guerra@fpct.ulpgc.es

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List of Acronyms

Acronym	Meaning
ACO	Asymmetrically Clipped Optical
AFE	Analog Front End
AM	Angle Magnifier
APD	Avalanche Photodiode
AWGN	Additive White Gaussian Noise
BB	Base Band
BER	Bit Error Rate
BP	Believe Propagation
bpc	Bit Per Colour
BSU	Beam Steering Unit
CAP	Carrier-less Amplitude and Phase
CPC	Compound Parabolic Concentrator
dB	Decibel
DAC	Digital-to-Analog Converter
DC	Direct Current
DCO	DC biased Optical
DFE	Digital Front End
DMT	Discrete Multi-tone
EIRP	Effective Isotropic Radiated Power
EM	Electro Magnetic
F/#	F Number
FEC	Forward Error Code
FFT	Fast Fourier Transform
FMC	FPGA Mezzanine Card
FOV	Field of View
FPGA	Field Programmable Gate Array
FSPL	Free Space Path Loss
FWF	Fiber-Wireless-Fiber
Gbps	Giga bits per second
HMD	Head Mounted Display
ICI	Inter Channel Interference
IFFT	Inverse Fast Fourier Transform
IM/DD	Intensity Modulation / Direct Detection

IR	InfraRed
LDPC	Low Density Parity Check
LED	Light-Emitting Diode
LO	Local Oscillator
MAC	Medium Access Control
MCRT	Monte Carlo Ray Tracing
MCS	Modulation and Coding Scheme
MMF	Multi-mode Fiber
NF	Noise Figure
NRZ	Non Return to Zero
OAM	Orbital Angular Momentum
ODH	Optical Detector Head
OFDM	Orthogonal Frequency Division Multiplex
O-OFDM	Optical OFDM
OWC	Optical Wireless Communication
OWIR	Optical Wireless Impulse Response
OOK	On-off Keying
PoC	Proof of Concept
PDF	Probability Density Function
PHY	Physical layer
PSD	Power Spectral Density
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
SC	Successive Cancellation
SCL	SC List
SINR	Signal to Interference plus Noise Ratio
SISO	Single Input Single Output
SLM	Spatial Light Modulator
SMF	Single Mode Fiber
SNR	Signal to Noise Ratio
SP	Sum Product
THF	Tremendously High Frequency
TIA	Transimpedance Amplifier
TIR	Total Internal Reflection
VGA	Variable Gain Amplifier

VLC	Visible Light Communications
VR	Virtual Reality
VSWR	Voltage Standing Wave Ratio
WORTECS	Wireless Optical/Radio TErabit CommunicationS
WDM	Wavelength Division Multiplexing

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1 Introduction

1.1 Context presentation

In future VR equipments, the need of data throughput will reach hundreds of Giga bits per second as described in the WORTECS D2.3a document. Furthermore, the VR experience should improve greatly if cables between the computer and the HMD are suppressed.
The goal of the project is to realise this high data rate connection using a wireless transmission system based on both radio and optical technologies.

> *Reality is a scientific and technical domain that uses computer science and behavioural interfaces to simulate in a virtual world the behaviour of 3D entities, which interact in real time with each other and with one or more users in pseudo-natural immersion via sensorimotor channels.*

Figure 1 - A CAVE-like environment (left) and an HMD (right).

1.2 VR requirement

1.2.1 Location

One of the key point to ensure a good VR user experience is the localisation (also called tracking). It consists of measuring on one side the position of the user in a delimited area, and in the other side, the orientation of the user head. More these information are precise and frequently sent, more the VR scene could be realistic and in phase with the user movements.
Autonomous system based on accelerometers could be used. A first calibration is done at the system set up, and the next position could be computed by integrating the accelerometers measures. But the too noisy measures obtained with low cost accelerometers introduce a bias in the position computation. By the way, a perceptible deviation of the position requires a recalibration quiet often.
This recalibration is done with an external equipment that capture the position of the HMD. The merge of the accelerometers and recalibration information gives a precise measure of localisation and orientation.
Two kinds of external tracking system exist: Inside-out and outside-in tracking.
The first one (inside-out) consist of catching static markers placed on the external environment using a camera mounted onto the HMD. From the markers position, the HMD can compute its own position information.
The second one (outside-in) consist of catching HMD pictures with many static cameras located all around the VR room, and compute its location.

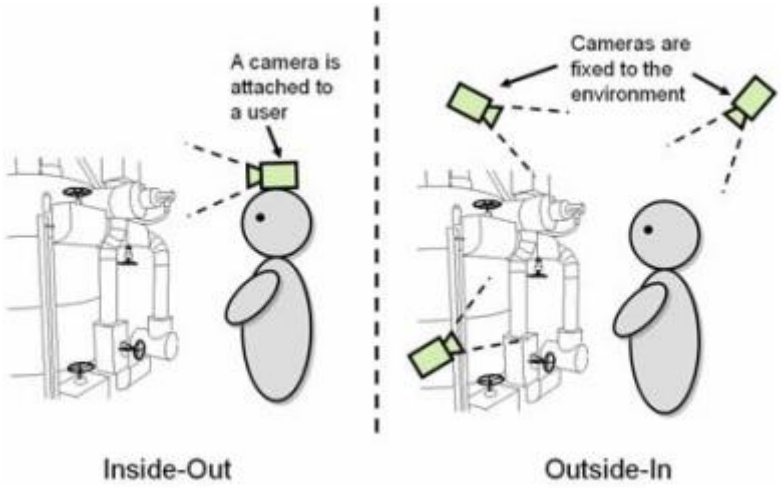


Figure 2 - Inside-Out and Inside-In location mechanisms example.

The location system available for the use case (SteamVR) is an evolution of the inside-out position tracking system. To avoid analysing the video captures inside the HMD (and by doing so save computing power), the camera has been replaced by IR sensors, and the fixed markers by an IR source.
The fixed marker is named base station or lighthouse. The base station generates two kinds of IR light. The first one is an omnidirectional flash, and is a kind of start of measure signal. The second one is based on a laser source. This source scan the user space as a scanner could do. One phase consist in scanning horizontally the user space using vertical laser line, and another phase consists in scanning vertically the user space using horizontal laser line.
When an IR receptor get the starting flash, it resets a time counter, and when it receives the horizontal laser (moving from up to down), it stops the time counter. Depending on the measured time, knowing the base station scanning velocity and its localisation, it is possible to compute the vertical plan where the captor is located.
Additionally, when an IR receptor gets the starting flash, it resets a time counter, and when it receives the vertical laser (moving from left to right), it stops the time counter. Depending on the measured time, knowing the base station scanning velocity and its localisation, it is possible to compute the horizontal plan where the captor is located.
The mix of these two information gives a line the receptor is located on, and by extension the lines where all receptors are located (30 of them). Combined with the well-known HMD geometry, an initial calibration phase and the 6 degree of freedom accelerometers embedded in the HMD, it is possible to track the HMD localisation and orientation with a precision of 2mm.
On a small cave, a single base station could be enough, but if the user is too far from it, or if the HMD is not well oriented, it could be possible that it does not have a direct view of the base station, and then loss the tracking capabilities. In order to avoid these situations, a second base station is installed on the opposite corner of the cave. The two light sources are synchronised to ovoid cross interferences, and the covered area could be expanded.

1.2.2 Virtual scene creation

In virtual reality, all the scenes sent to the HMD are fully live generated by a computer. Based on the location of the user in the room, the computer defines a new scene each time the user is moving. For each new scene, two new pictures are computed (one for each eye). These pictures are not fully defined, they are only meshed in order to be generated as fast as possible (90Hz). These meshes are sent to the graphic card which have the responsibility to apply on it all the advanced algorithm (and heavy computing process) to create textures, light reflexions and others features that makes the picture realistic. The video signal generated is sent to the HMD using standard connection like HDMI or Display ports. Both of them have been created for the transport of first digital video signals and there maximum bandwidth has been upgraded along the generation.

1.2.3 Connectors standards data rate and throughput

The two main standards that can be used in virtual reality are the HDMI and the Display Port. Their capacity has been improved over the years and their maximum throughput and data rate evolutions are presented in the table here after.
In parallel, different video resolutions are presented, from the simple HD video format till the 8K advanced video format, and their associated data rate are computed. The table clearly show the maximum video resolutions that can be transport by each standard revision.

Remark: For the data rate definition, uncompressed 8 bpc (24 bit/pixel) colour depth with RGB or $Y'C_BC_R$ 4:4:4 colour format and CVT-R2 timing are used. Uncompressed data rate for RGB images in bits per second is calculated as bits per pixel × pixels per frame × frames per second. Pixels per frame include blanking intervals as defined by CVT-R2.

Video Format				HDMI					DP			
				Version / Max Throughput / Maximum Data Rate / Serdes Coder					Version / Maximum Data Rate / Serdes Coder			
				1.0–1.1	1.2–1.2a	1.3–1.4b	2.0–2.0b	2.1	1.0–1.1a	1.2–1.2a	1.3	1.4
				4,95	4,95	10,2	18	48	10,8	21,6	32,4	32,4
Shorthand	Resolution	Refresh Rate (Hz)	Data Rate Required[a]	3,96	3,96	8,16	14,4	42,6	8,64	17,28	25,92	25,92
				8b/10b	8b/10b	8b/10b	8b/10b	16b/18b	8b/10b	8b/10b	8b/10b	8b/10b
720p	1280 × 720	30	720 Mbit/s	Yes	Yes	Yes	Yes	Yes				
		60	1.45 Gbit/s	Yes	Yes	Yes	Yes	Yes				
		120	2.99 Gbit/s	No	Yes	Yes	Yes	Yes				
1080p	1920 × 1080	30	1.58 Gbit/s	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
		60	3.20 Gbit/s	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
		120	6.59 Gbit/s	No	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes
		144	8.00 Gbit/s	No	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes
		240	14.00 Gbit/s	No	No	No	Yes	Yes	No	Yes	Yes	Yes
1440p	2560 × 1440	30	2.78 Gbit/s	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
		60	5.63 Gbit/s	No	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes
		75	7.09 Gbit/s	No	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes
		120	11.59 Gbit/s	No	No	No	Yes	Yes	No	Yes	Yes	Yes
		144	14.08 Gbit/s	No	No	No	Yes	Yes	No	Yes	Yes	Yes
		165	16.30 Gbit/s						No	Yes	Yes	Yes
		240	24.62 Gbit/s	No	No	No	No	Yes	No	4:2:2[c]	Yes	Yes
2160p (4K)	3840 × 2160	30	6.18 Gbit/s	No	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes
		60	12.54 Gbit/s	No	No	No	Yes	Yes	No	Yes	Yes	Yes
		75	15.79 Gbit/s	No	No	No	No	Yes	No	Yes	Yes	Yes
		120	25.82 Gbit/s	No	No	No	No	Yes	No	4:2:2[c]	Yes	Yes
		144	31.35 Gbit/s	No	No	No	No	Yes	No	No	4:2:2[c]	DSC[d]
		240	54.84 Gbit/s	No	No	No	No	Yes[b]	No	No	4:2:0[c]	DSC[d]
5K	5120 × 2880	30	10.94 Gbit/s	No	No	No	No	Yes	No	Yes	Yes	Yes
		60	22.18 Gbit/s	No	No	No	No	Yes	No	4:2:2[c]	Yes	Yes
		120	45.66 Gbit/s	No	No	No	No	Yes[b]	No	No	4:2:0[c]	DSC[d]
8K	7680 × 4320	30	24.48 Gbit/s	No	No	No	No	Yes	No	4:2:2[c]	Yes	Yes
		60	49.65 Gbit/s	No	No	No	No	Yes[b]	No	No	4:2:0[c]	DSC[d]
		120	102.2 Gbit/s	No	No	No	No	Yes[b]				
Video Format				1.0–1.1	1.2–1.2a	1.3–1.4b	2.0–2.0b	2.1	1.0–1.1a	1.2–1.2a	1.3	1.4
				HDMI Version					DisplayPort Version			

Table 1 - DP and HDMI video standards data rate and throughput

The HDMI2.0b and display port 1.4 are the standards used nowadays. The HDMI2.1 is still under standardisation, and products supporting it are not ready yet.

1.2.4 HMD resolution

As described in the D2.3a document, if we consider that

- the standard human eye resolution is one arc minute (it can distinguish details as small as one sixtieth of a degree)
- the eye field of view is 150° for each, with an overlap of 90° (the overall FOV is about 210°)
- a normal head speed reach 120°/s,

The required row bandwidth of a non-limiting HDR HMD would be 470Gbps.

1.2.5 Overall latency

To ensure a good user experience, the total amount of time measured from the head movement, until the final display of the new corresponding scene must be smaller than 17 ms. To avoid seasick troubles, this latency must be smaller than 20 ms.
This latency includes:

- HMD movement detection
- new location definition
- location transfer to the computer
- scene generation
- scene transfer to the HMD
- scene display

Taking into account that a classical VR system has a typical motion to photon latency of 15ms (MTP) implies that only 2 ms can be added to the system when replacing the cables by the wireless system.

1.3 Wireless VR

The goal of wireless VR is to replace the two links between the computer and the HMD with wireless system. The first one is the uplink cable, which is a USB cable that carries the localisation information from the HMD and the computer. The second one is the downlink cable, which is a video cable (HDMI or Display Port depending on the HMD used) that carry the VR scene from the computer to the HMD.
The following Figure 3 represents the two links between computers and the HMDs in the case of a two-user scenario.

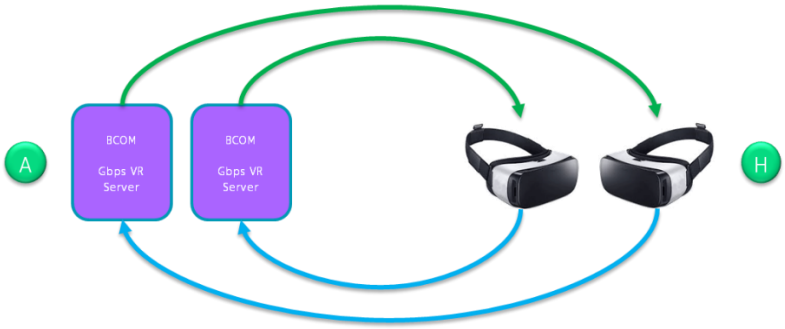


Figure 3 - Wired VR overview.

The Downlink cable (the green one) carries the high throughput video from the b<>com server (point A) to the HMD (point H). Depending on the HMD display used and the cable's maximum capacity, the video data rate could reach 32 Gbps.
The Uplink cable (the blue one) carry the low throughput localisation information from the HMD (point H) to the b<>com server (point A). The connection used is based on USB standard, release 2.0 or 3.0 depending on the HMD used. However whatever the maximum cable bandwidth, based on the D2.3a results, the location data rate would be smaller than 1Mbps if no information other than localisation is sent back.
Considering that two wireless transmission systems are used, a MAC layer be in charge of delivering data from the computer to the most appropriated system depending on the quality of each of them. Furthermore,

considering that multiple users could operate in the same time, data sent by the computers (one computer per user) will be associated to a destination mac address (one address per HMD). This way, multiple sources could send video data to multiple users through radio or optical link.
The interconnection of equipment to a MAC layer using an IP interface is not a problem when data transmission is IP based. However in our system, none of the two targeted HMDs are IP ready. The HMD is fed by the graphic card of the computer with a video signal, transported by a video link, using a video standard (HDMI or DP). A direct interconnection from video connector to IP one is impossible. That is why an additional module will be in charge to make this connection possible.
Here after, the overall scheme of what could be the multi user wireless VR system is detailed.

In Figure 4, going from point A to H, the video signal will follow the next steps:
- From A to B : The video data is converted into IP packets
- From B to C : The IP packets are oriented to the best transmitter
- From C to D : IP data is encoded mapped and sent onto the air (optical or radio)
- From D to E : The channel transport the data
- From E to G : Received signals are de-mapped, decoded and sent as IP packets
- From G to H : IP packets are converted into video signal

Similarly, going from point H to A, the localisation signal will follow the next steps:
- From H to G : Localisation data is converted into IP packets
- From G to F : The IP packets are oriented to the best transmitter
- From F to E : IP data are encoded, mapped and sent onto the air (optical or radio)
- From E to D : The channel transport the data
- From D to C : Received signals are de-mapped, decoded and sent as IP packets
- From C to B : IP packets are sent to the corresponding destination
- From B to A : IP packets are converted into localisation data

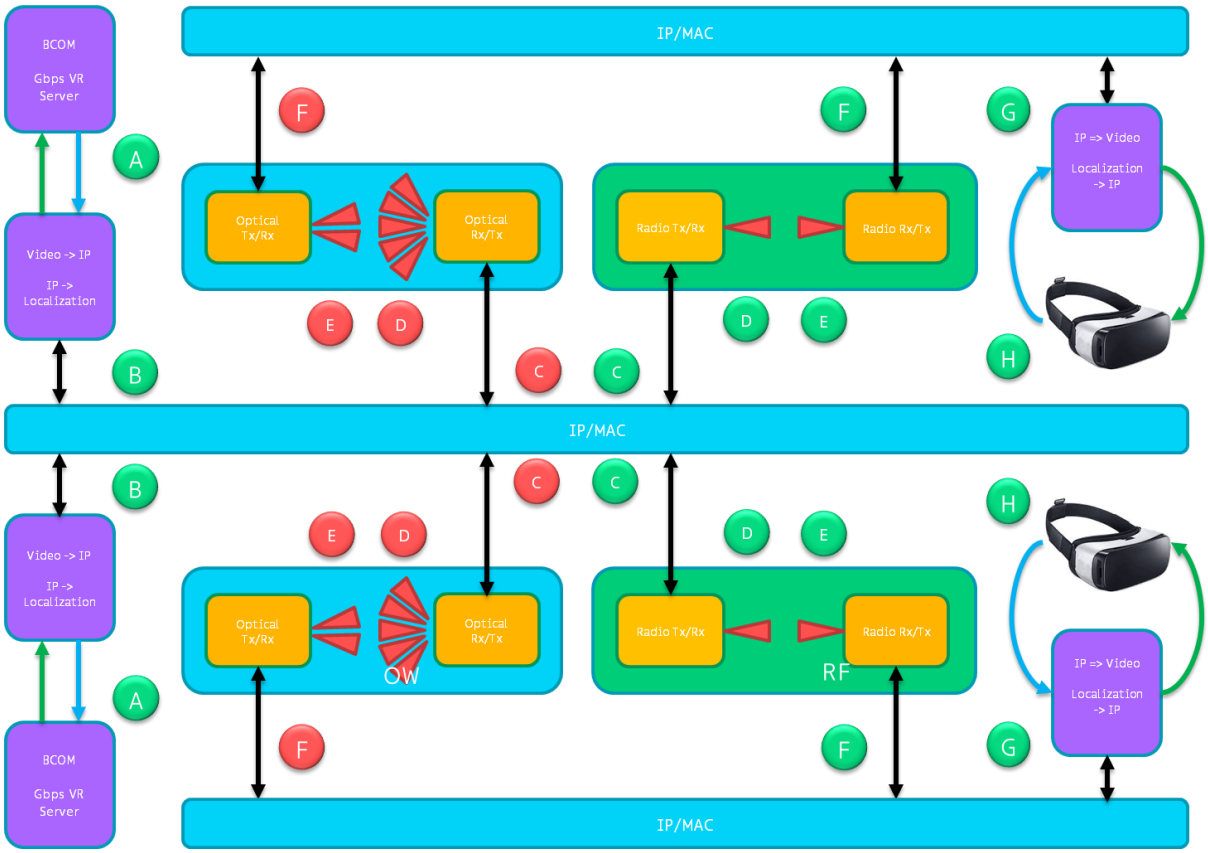


Figure 4 - Wireless VR overview

1.4 State of the art

As described in the D2.3a, few VR wireless products already exist. They are developed for SoTA HMD, with resolution of 2x1080x1200 and frame rate of 90Hz. The corresponding throughput of 5.6Gbps (see 2.1.1) is transmitted aver the air using 802.11ac or 802.11ad standards.
In the case of the 802.11ac transmission, the available bandwidth of 1Gbps is not enough and compression is mandatory.
In the other cases, compression can be avoided thanks to the larger available bandwidth.
The problem with the video compression is the time consumed to compress on one side, but most of all, the time used to decompress on the other side. That explains why the systems based on 1Gbps bandwidth have a latency of 12ms.

Name	Protocol	Bandwidth	Latency	Max Resolution
TPCast	Proprietary?	7 Gbps?@60 GHz	<2ms	2x1080x1200@90Hz
Kwik VR	802.11ac	1 Gbps@5 Ghz	<12ms	2x1080x1200@90Hz
Immersive VR	802.11ac & 802.11ad	7 Gbps@60 GHz	1ms	4K (lossy 20:1)
NGCodec	802.11ac	1 Gbps@5 Ghz	<12ms	2x1080x1200@90Hz (lossy 500:1)
Nitero	802.11ad	7 Gbps@60 GHz	1ms	2x1080x1200@90Hz

Table 2 - Wireless VR solutions

2 Demonstration set up

2.1 Hardware set up

A selection of the VR elements in high-end components was made, keeping in mind their realistic availability for the project deadline.

2.1.1 Current generation HMD

The classical HMDs available the market are the HTC vive and the Oculus rift. These HMDs use a single display, which has a total resolution of 2160x1200 pixels with a refresh rate of 90 Hz. This single display provides to each eye a picture of 1200x1080 pixels.
With 8 bit per colour definition, the equivalent throughput of this screen is 5.2Gbps.

HMD Name	**Resolution**	**Raw Bandwidth**	Comment
HTC Vive	1x2160x1200@90Hz	5.6 Gbps	Already available at b<>com
Oculus Rift	1x2160x1200@90Hz	5.6 Gbps	

Table 3 - State of the art HMDs

2.1.2 Next generation HMD

Few month ago, a new generation of HMD arrived on the market.

- Their resolutions are greatly improved when compared to the state of the art and reach 2560x1440 on each eyes.
- The Field of view is close to the ideal one and reaches 210°.

2.1.2.1 StarVR

One of them is the StarVR, developed by Starbreeze. With a resolution of 2x2560x1440, it outperforms the SoTA HMD both in term of resolution and of field of view. Unfortunately, this company has signed a partnership with IMAX and therefore, integrating this product in the project seems to be difficult.

2.1.2.2 Pimax8K

Another HMD of new generation is the PiMax8K, result of a Kickstarter campaign, and should be available at end of 2018. Its name comes from the definition of the screens used for each eyes. Each of them is a 4K definition screen (8K for 2x4K).
Each screens have a definition of 3840x2160 pixels. They announced a frame rate of 90Hz, a time to display of 15ms, and the couple offer a field of view of 200° horizontally and 120° vertically.
Nevertheless, the problem with such a high definition screens with high frame rate is computing power required to create live scenes. Effectively, even high end GPU cards are not able to generate two 4K pictures at 90 Hz. For this reason, this HMD has been equipped with an interpolation system which upscale incoming pictures from a resolution of 2560x1440 to the required 4K resolution. Finally, the generated VR scene would have the same resolution as the StarVR HMD.
The following table present the definition and the bandwidth of the new generation of HMD, still considering 24 bits per pixel (8 bits per colour).

HMD Name	**Resolution**	**Raw Bandwidth**	Comment
Pimax8K	2x3840x2160@90Hz	15.9 Gbps	Image upscale from 2x2560x1440 to 2x3840x2160
StarVR	2x2560x1440@90Hz	15.9 Gbps	

Table 4 – New generation HMDs

For the video transport, the HMD is connected to the graphic card using a DisplayPort1.4 connector. The location information is transmitted to the computer using a USB3.0 connector.
The SteamVR tracking system is supported by the Pimax8K HMD. A custom tracking system is also planned but not available yet.

Field of view	200° Horizontally, 120° Vertically
Resolution	2x3840x2160 (Image upscale from 2x2560x1440)
Screen	Customized low persistence liquid (CLPL) display
MTP (Motion to picture) Latency	15ms
Refresh rate	75/90 Hz per eye (Support 150/180 Hz with Brainwarp)
Interface	DP1.4, USB 3.0

Table 5 – Pimax8K technical specifications

2.1.3 GPU based Computer

The generation of ultra-high definition VR scenes at a high refresh rate requires a powerful computer. Such a computer is called a VR Ready computer.
In case of classical HMD, with a resolution of 2160x1200@90Hz, the computer could be composed of the following:

- A mother board, powered with a Core i5 processor
- 8 GBytes of RAM
- A graphic card NVidia GTX 980 or 1070

In case of new generation HMD, the computer should be composed with the following:

- A mother board, powered with a Core i7 processor
- 16 GBytes of RAM
- A graphic card NVidia GTX 1070 or 1080, and eventually two of these (using SLI) if full 8K is generated.

Finally, Unity is used as the application software. It creates and animates the scene depending on the user location and movements.

2.1.4 Localisation system

As the SteamVR tracking system is already installed on the b<>com smart cave, and as the Pimax8K is SteamVR compatible, it will be the tacking system of the project use case.

2.1.5 Connectors

The targeted HMD should be the Pimax8K. Therefore, the connectors used between the graphic cards and the display will be:

- DP1.4 for the video transport
- USB3.0 for the localisation information transport

2.2 Environment description

2.2.1 The Smart Cave

The VR environment (named the smart cave) is the area where the user can move during its virtual word exploration. The cave structure is made of metallic tubes of 5 cm diameter which are linked in groups of four. Floor and ceiling are made out of green painted wood and a long piece of green fabric is hanging all around the four walls.
A 3D model of the complete smart cave has been realised for wave propagations and channel estimations studies and the following Figure 5 gives an overview of it.

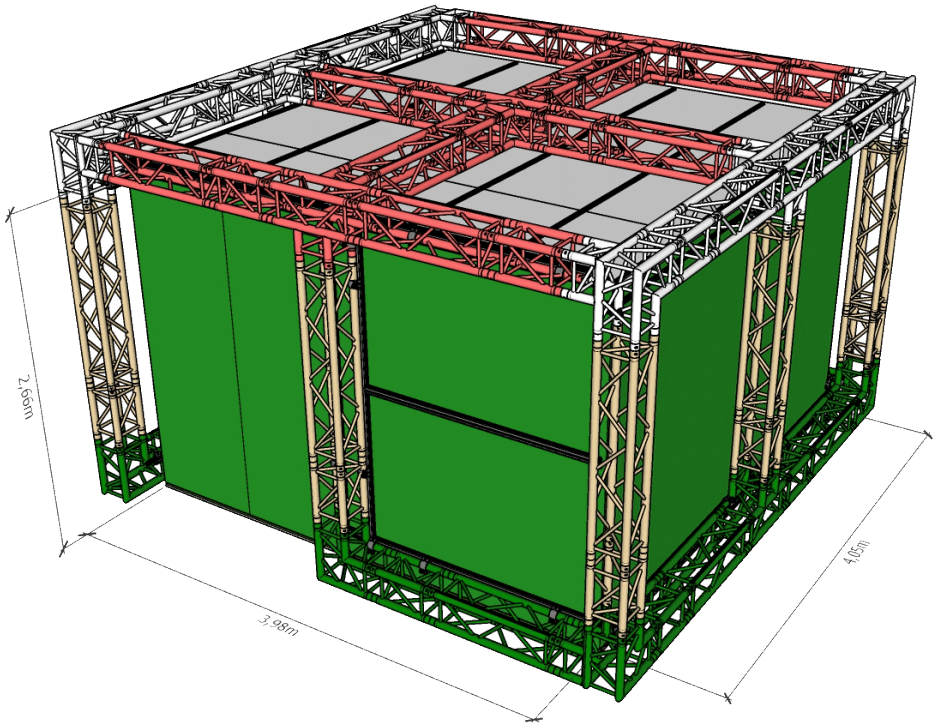


Figure 5 - Cave structure and dimension

2.2.2 The show room

The smart cave is installed in a dedicated show room on the ground floor of b<>com building. It is used for virtual reality demonstrations performed by the HyperMedia division.
The walls, floor and ceiling are mainly made of concrete, and many windows are placed all around the room. The dimensions of the show room are 7 m wide by 20 m long and 3.6 m high.
The following figures are extracted from its 3D model.

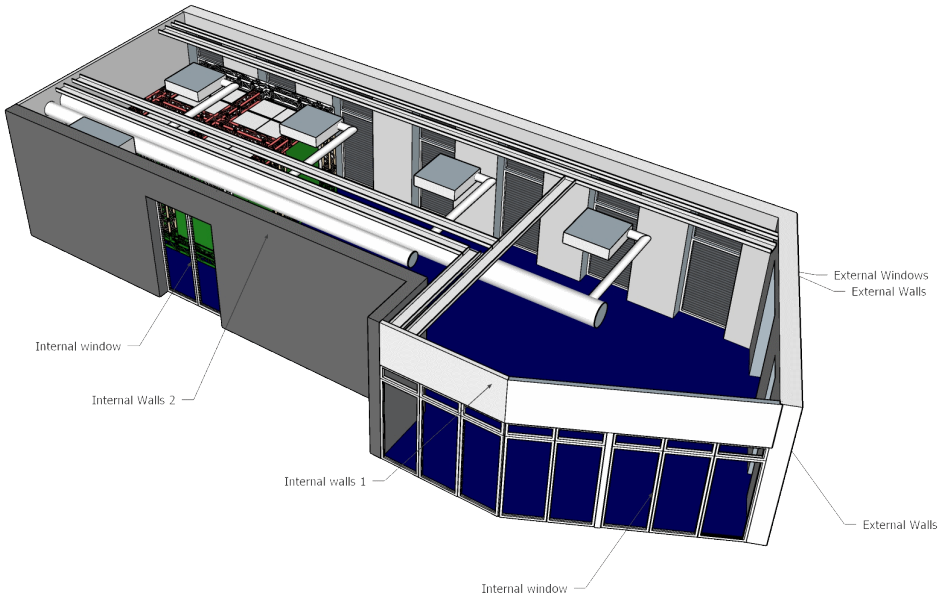


Figure 6 - Showroom front view

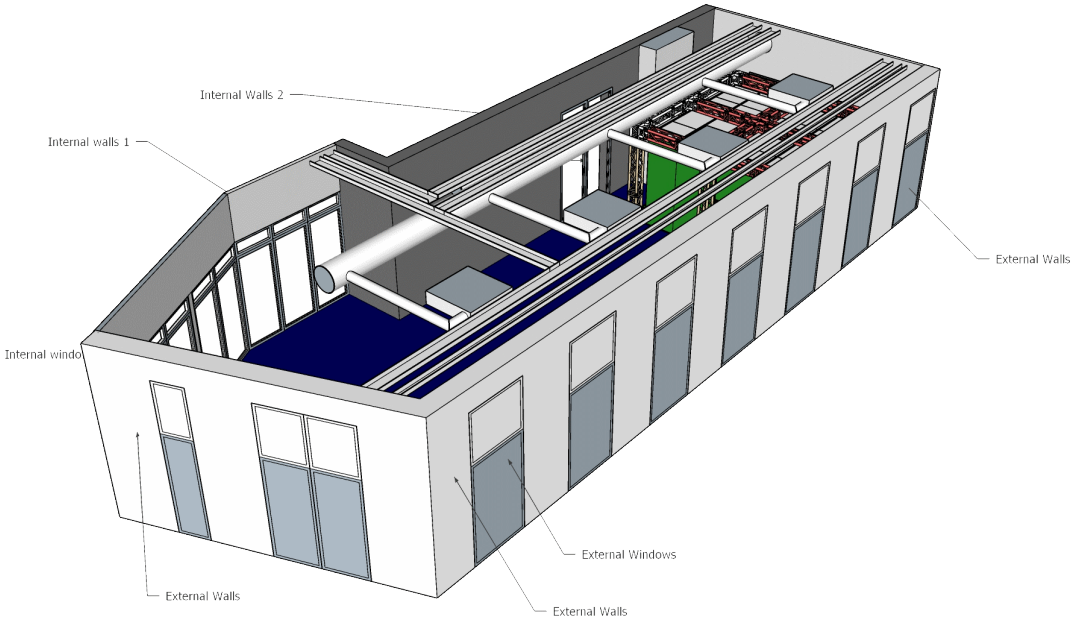


Figure 7 - Showroom back view

The smart cave is located in the back of the thinnest part of the showroom as can be seen on previous figures.

2.3 Channel modelling

Indoor Optical Wireless Impulse Response (OWIR) modelling and simulation is a well-investigated subject, since it determines the main communication channel's restrictions and capabilities. In this kind of scenario, the main factors that affect the impulse response are the geometrical parameters of the link (emitter and receiver positions, and the scenario's geometry), and the physical parameters of the materials involved in the propagation (primarily their reflectivity-wavelength response $\rho(\lambda)$. Since the working wavelength is small enough compared to the objects within the scenario, geometric optics can be used to simulate the OWIR. Furthermore, by the same reason, diffraction can be neglected.
Monte Carlo Ray Tracing (MCRT) is the most extended simulation method in OWC. In its modified variant, random directions are generated following the normalized emission pattern as Probability Density Function (PDF), enhancing the convergence since the most significant contributing rays are calculated [1].
Generally, the materials involved in an indoor environment present a linear behaviour in terms of wavelength. When light from a determined wavelength impinges on a surface, part of the energy is absorbed and the rest is reflected to the medium. This reflection can be diffuse (Lambertian), quasi-specular (Phong, Torrance, LaFortune) or fully specular (Snell) [2]. However, there also exist some materials which present a nonlinear behaviour as in phosphor materials or wavelength-dependent reflecting surfaces, which consist on a change of wavelength after the impact. The incident energy is not only spatially scattered, but also frequency distributed (always to longer wavelengths), as is the case of phosphors or plastics [3] that are now being extensively used in sport clothing. In a general way, there is an incident-angle-and-frequency dependent function $\rho(\theta_i,\lambda,\lambda')$ that models this phenomenon. However, since the materials involved in the demonstration environment present linear and simple reflection patterns, the simulation has not included this degree of complexity.
In OWC, the indoor channel does not present frequency-dispersive behaviour, and pulse broadening due to it does not occur. This is not the case of THF, in which there is a great difference between wavelengths (frequencies). Furthermore, in OWC IM/DD is used and hence there is no interest in the signal's phase. On the other hand, in THz-RF, destructive and constructive interference may occur and the phase has to be taken into account. Regardless this difference, in this project a joint RF/OWC simulation procedure has been proposed.

2.3.1 Joint RF/OWC simulation model

As mentioned above, there are slight differences between THz-RF and OWC regarding indoor propagation. However, it has been stated that MCRT algorithms can be used in both cases. In this subsection, the model proposed for WORTECS is presented. The implemented software accepts a triangularized .OBJ file as 3D model input. This file type is standard and most 3D modelling software is able to export the models to it.

Furthermore, a materials file binding each material name in the .OBJ file and the corresponding reflection pattern is defined. Finally, a file in which the simulation parameters (number of rays, number of rebounds, receiver locations, etc.) are set, is also needed as input to the channel's impulse response simulation application.
The model is based on three main stages (Figure 8):

- **Pre-processing.** During this stage, the scenario is inflated from the configuration files and the 3D object file (.OBJ). Additionally, and optionally, pre-processing in a Computer Graphics-fashion can be performed (shadow precomputing, enclosing boxes, etcetera). Due to the simplicity of the scenario under consideration, this last part has not been included.
- **Ray Tracing.** This is the geometrical part of the algorithm. A "forced" LOS contribution is always computed in first place from each emission point (source and surface impact points). Following, the rays are generated using a uniform distribution (Modified MCRT should not be used, this will be commented later), and the contributions are calculated simultaneously on all the defined receiving points. Each ray impacting the receiver point comprises the direction, intensity per square meter (complex-valued), travelled distance and followed trajectory. All the rays are stored in a list-based structure in which each index is associated to a delay.
- **Post-processing.** In this stage, the rays are processed to conform the impulse response. Since the MCRT algorithm returned a ray distribution in terms of incidence angle and irradiance, a receiver object must be defined. In the case of an OWIR, it will be defined by a lens system (FOV, lens gain and photo-receiver area). In the case of a THz-RF receiver, it will be described by its antenna gain angular distribution and antenna size. Once the receiver pointing direction is defined, the irradiance is converted to the actual received power and the impulse response is conformed.

Figure 8 - Stages of the developed algorithm

Mathematically, the impulse response comprises the contributions of all the arriving rays as shows Equation 1.

$$h(t,\Psi) = \sum_i P(\theta_i)\, R(\Psi_i)\delta(t-\tau_i) \prod_j L_j\, e^{\alpha(\lambda)d_j - j(kd_j + \phi_j)} \qquad (1)$$

In (1), i is the arriving ray index, $P(\theta_i)$ is the output power per steradian and square meter at angle θ_i , $R(\Psi_i)$ is the receiver gain at the incidence angle Ψ_i, τ_i is the ray's delay, j is the rebound index, L_j is the loss suffered at the j-th impact, $\alpha(\lambda)$ is the attenuation due to the EM interaction with the medium, d_j is the sub-link's travelled distance, k is the wavenumber and ϕ_j is the rebound-induced phase shift, which is generally statistical. Note that the obtained impulse response depends on the incident angle. Figure 9 depicts how the MCRT calculation is performed.

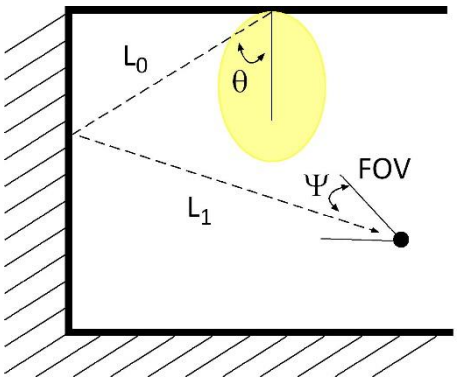


Figure 9 - Description of the scenario

Depending on the emission bandwidth, the effect of $\alpha(\lambda)$ may or may not be significant. In the case of narrowband signals, Equation 1 is enough, but for broadband signals the impulse response must be split into several sub-responses taking into account the effects of the frequency-dependent attenuation.
The current version of the impulse response estimator performs the calculation simultaneously on all the pre-defined receiver positions. Each time a rebound occurs, "forced" contributions are calculated taking into account the emitter's gain (reflection pattern or emission pattern, depending on the case) for all the receiver points. Each receiver has its own data structure in which the following information is stored:

- **Arrival time**. This is the travelled distance divided by the speed of light.
- **Angle of arrival**. This is important since it provides flexibility for the post-processing stage.
- **Power surface density**. The irradiance in [W/m^2] each ray carries (complex-valued).

In this version, the trajectory is not stored since it will be an optimised version of the software. This optimisation will allow a generalization of the Ray Tracing output. Using the same geometry and Ray Map, the impulse responses at the receivers could be calculated changing the physical parameters of the surfaces and emitters (reflectance, wavelength and emission pattern).
Depending on the domain type (RF of OWC), the final impulse response would be calculated using Equation 2 or 3.

$$h^{OWC}(t) = \sum_{\Psi_j \in FOV} \left|h\left(t, \Psi_j\right)\right| A_{pd} \cos \Psi_j \quad (2)$$

$$h^{RF}(t) = \sum_{\Psi_j \in FOV} h\left(t, \Psi_j\right) A_{rx} \cos \Psi_j \quad (3)$$

It must be taken into account that in the case of RF, the obtained impulse response is the complex envelope. Since MCRT is time consuming, this approach allows an easy, flexible and quick way to test different types of receiver. With the obtained impulse response map, both channel gain (inverse of the link loss) and bandwidth can be evaluated at every point of the scene.
The next subsection shows some simulation results inside b<>com's Smart Cave. These results are focused on the OWC part, since it is the Agreement's priority, but will be also obtained for the RF part if the schedule allows it.

2.3.2 Smart Cave OWIR results

At this stage of the project, only OWIR has been obtained. Due to this, the emission pattern of the light source has been fixed and a Modified MCRT has been used to improve the convergence. The final objective, if the timetable allows it, is developing a generalized RF-OWC compatible version independent of the source's emission pattern. In that case, the trajectory must be stored and the weights of Equation 1 will be calculated at the post-processing stage.
In this first stage, the simulations have been focused on the available hardware, whose characteristics can be observed in Table 6 [4]. Regarding b<>com's Smart Cave, the material optical reflectance have been consulted in the literature, and their responses are available in Table 7. Figure 10 - Top view of b<>com's Smart CaveFigure 10 shows a schematic version of the scenario.

Emitter:	**Light source type**	De-coherenced laser + diffuser
	Wavelength	860 nm
	Nominal optical power	19 dBm
	Estimated lens+diffuser losses	2 dB
	Output radiation pattern	Generalized Lambertian (m = 20)
Receiver:	**Type**	APD + Concentrator
	FOV	30º
	Responsivity (at 860 nm)	0.5
	Avalanche gain	100
	Rise time	1.4 ns
	Active Area	3 mm^2
	Concentrator material	PMMA

Table 6 - Emitter and receiver characteristics

Material	**Reflectance @860 nm**	**Reflection pattern**
Cotton + green dye	0.65 [5]	Lambertian
Plywood + white paint (TiO_2)	0.85 [6]	Lambertian

Table 7 - Reflectivies of the Smart Cave's materials

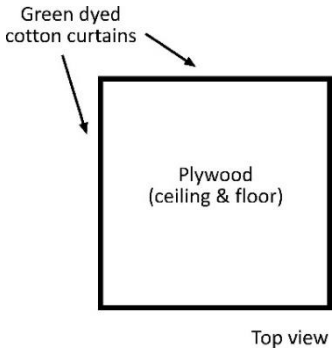


Figure 10 - Top view of b<>com's Smart Cave

The simulated points are located at 1.5 meters from the ceiling, with the emitter pointing downwards at the centre of the cave's ceiling. Two simulations were performed, the first one with a hypothetical receiver pointing upwards and a second one perfectly pointing to the emitter. Figure 11 and Figure 12 depict the result for SNR and Bandwidth respectively. The observed high available bandwidth is due to the small aperture angles of both emitter and receiver.

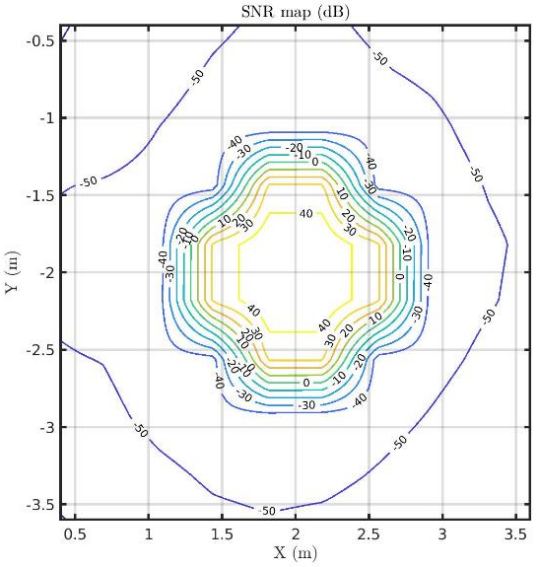


Figure 11 - SNR map for a Tx/Rx set described in Table 6. The link height is 1.5 meters.

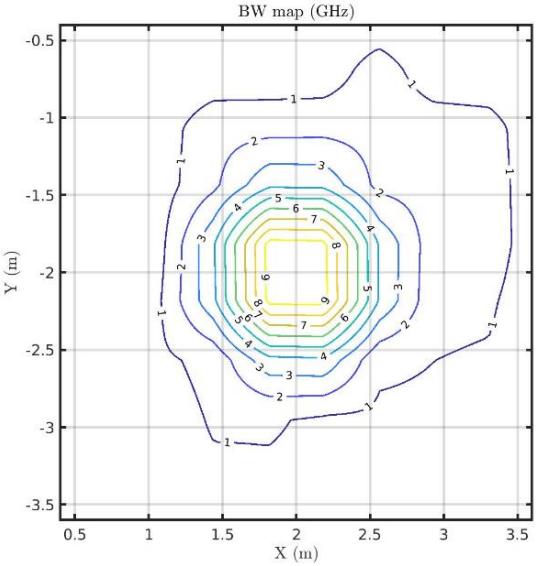


Figure 12 - Bandwidth (*x*,*y*) map for a receiver pointing upwards in GHz.

As a clarification, channel gain and bandwidth have been calculated using Equations 4 and 5 respectively.

$$H(0) = \sum_i h^{OWC}(t_i) \tag{4}$$

$$BW = 0.2 \left(\sum_i \frac{t_i^2 h^{OWC}(t_i)}{H(0)} - \left(\sum_i \frac{t_i h^{OWC}(t_i)}{H(0)} \right)^2 \right)^{-1/2} \tag{5}$$

For the SNR evaluation, the receiver characteristics of Table 6, obtained from [6] were introduced into the simulation. The result can be observed in Figure 13. From PLF, the minimum estimated SNR to appropriately decode the OFDM frames is 30 dB, which leads to a cell radius of about 0.65 m at that height. From the bandwidth simulations, it can be observed that the 200 MHz requirement is fulfilled at every location. In the next subsection, single ray simulations taking into account the link range and the random head movement of the user are presented.

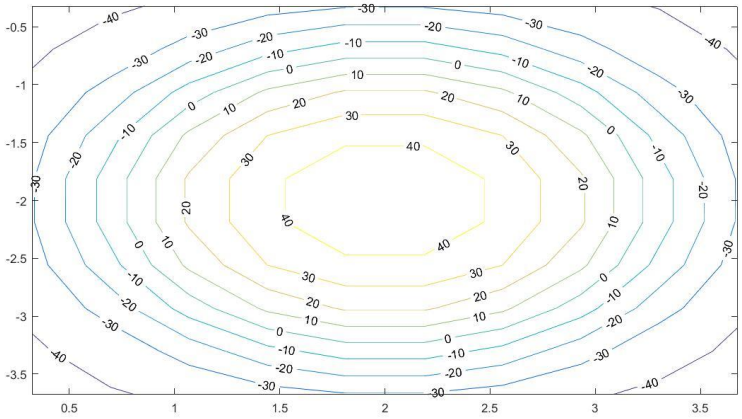


Figure 13 - SNR evaluation for a receiver pointing towards the emitter- cell radius ~0.5 m.

2.3.3 Cell radius estimation using statistical simulations

Once the bandwidth allocation of the link has been assessed by MCRT simulations, the random movement of the head must be taken into account to properly design the head-mounted optical receiver. For this purpose, the random head movement has been assumed as Lambertian with azimuthal symmetry for simplicity (Figure 14), although a more in-depth analysis of the literature will be made.

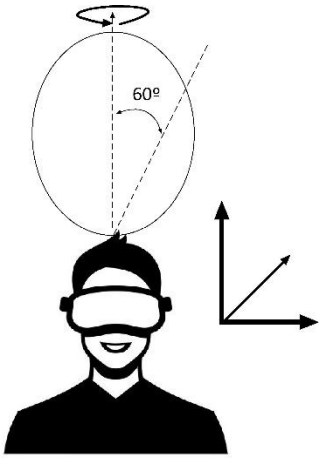


Figure 14 - Statistical approximation of the user's head attitude.

Figure 14 models as a Pure Lambertian distribution on elevation with azimuthal symmetry (uniform distribution).

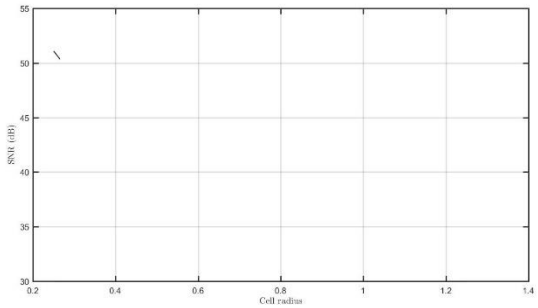
As a starting point, the restrictions to the first-approach demonstrator topology design are:

- Only 6 receivers are available
- Only 6 transmitters are available
- The optical characteristics of both emitter and receiver are immutable

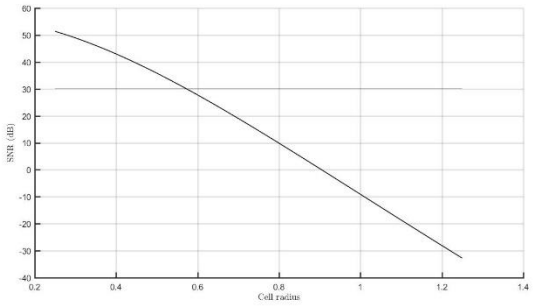
- The SNR must be higher than 30 dB [7]
- The link must work for a range between 1 and 2 meters

Since the demonstration area must be maximised to show the proof-of-concept design, it seems logical to assume in first instance that the cells will be single-emitter. From Figure 13, and re-evaluating the SNR at both 1 meter and 2 meters (Figure 15), it can be observed that the cell radius is FOV limited at very short distances for the closest link, and that in the best case, the cell would present 80 cm radius for the longest link. However, this simulation assumes a single receiver orthogonal to the ceiling, and a more realistic simulation must be performed. Figure 16 depicts the channel availability for a single receiver at the link range limits. The channel availability has been calculated as shows Equation 4. This estimation has been obtained using Laplace's formula for 1000 independent random runs of the head's attitude at each radial distance.

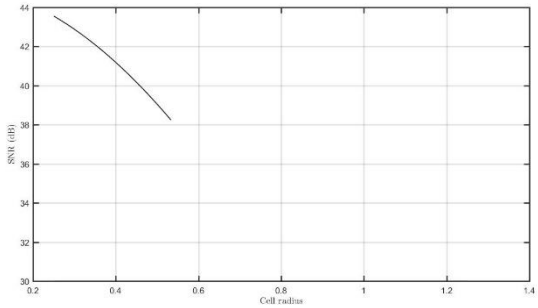
$$ChAv = p(SNR \geq 30\ dB) = \frac{Runs\ with\ SNR \geq 30\ dB}{Total\ runs} \quad (4)$$



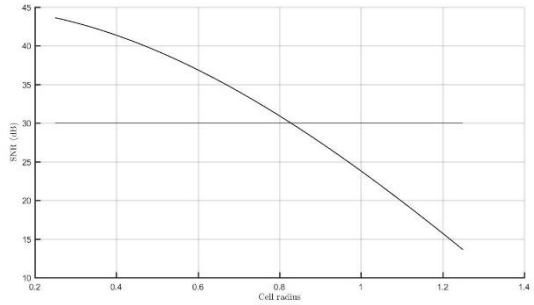
(a) SNR vs cell radius for a receiver pointing upwards



(b) SNR vs cell radius for a receiver pointing towards the emitter



(c) SNR vs cell radius for a receiver pointing upwards



(d) SNR vs cell radius for a receiver pointing towards the emitter

Figure 15 - SNR distribution for upwards-pointing receiver (left side), and best case scenario (right side). a) and c): 1 m link, b) and d): 2 m link.

It can be observed that this topology is not suitable to perform a reliable communication. At this point, two options arise. The first one is to develop a multi-receiver endpoint covering as much solid angles as possible, and the other one is to mount the photo-receiver over a stabilized platform.

The multi-receiver design and results are shown in Figure 16. It can be observed that using only 6 receivers the link cannot be ensured. On the other hand, in Figure 18 the stabilized-platform results using both single-receiver and multiple-receiver approaches are shown. As a clarification, the channel availability for the multi-receiver topology has been calculated considering that at least one receiver complies with the SNR requirement. It is straightforward to demonstrate that the reduced receiver's elevation (modelled as a Generalized Lambertian with m=180 – 10 degrees of FWHM) has a bigger impact on the link's availability than the placement of multiple-receivers. Table 8 shows the estimated cell radii assuming that 95% of channel availability is enough to establish a cell-radius limit.

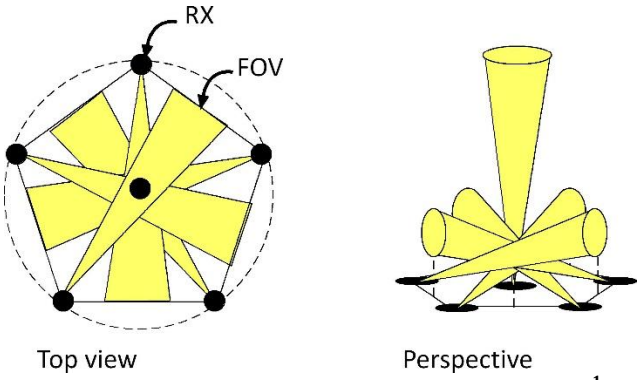
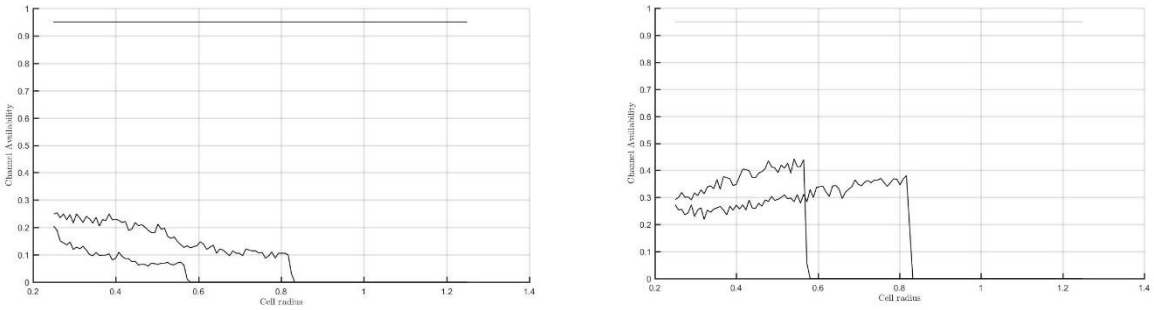


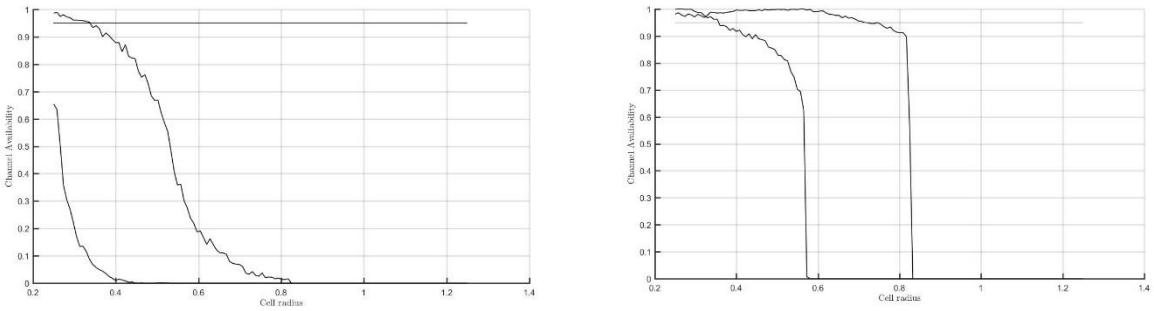
Figure 16 - Top view and perspective of the proposed multi-receiver topology[1].



(a) Channel availability using a single-receiver topology

(b) Channel availability using a multi-receiver topology

Figure 17 - Channel availability vs radial position for both single-receiver and multi-receiver topologies[2].



(a) Channel availability using a stabilized single-receiver topology

(b) Channel availability using a stabilized multi-receiver topology

Figure 18 - Channel availability vs radial position for the stabilized versions of the essayed topologies[3].

	Single receiver	**Multi-Receiver**
Short link (1 m height)	N/A	35 cm
Long link (2 m height)	35 cm	75 cm

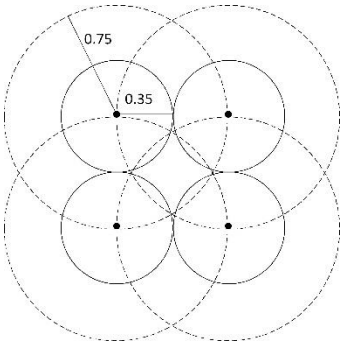
Table 8 - Estimated cell radii

With the cell radius estimate, the cell distribution must be analysed in order to define the best coverage taking into account possible interferences between adjacent cells. The next subsection describes the studied possibilities in this regard.

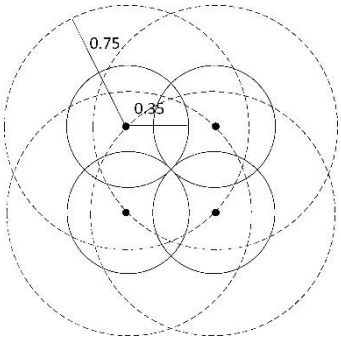
[1] Note that there are still uncovered solid angles due to the small amount of available receivers.
[2] The threshold has been fixed at 95% (horizontal line). The two curves on each graph correspond to the 1 m and 2 m links.
[3] Note that the single-receiver topology does not comply with the 95% of availability for the 1 m link, making necessary to include several receivers.

2.3.4 Analysis of the possible cellular distributions

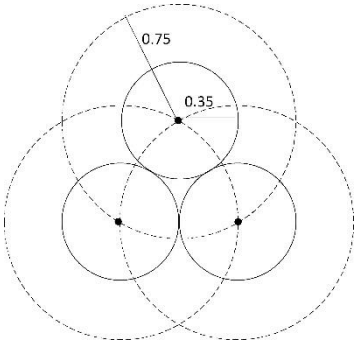
In the previous subsection, it was obtained that the radii for the height-variable links range from 35 cm to 75 cm. By taking into account that an average person needs approximately 75 cm of personal space to feel comfortable, the obtained results seem to be within the acceptable range. At this point, the cell distribution must be analysed in terms of covered area, fill factor and overlapping between adjacent cells. Currently, the obtained results only cover the geometrical part of the problem, but the next action is to study the effects of the overlapping on the SINR.
The studied cell topologies can be divided into triangular and rectangular, and also respect to the fill factor. Figure 19 shows the proposed distributions.



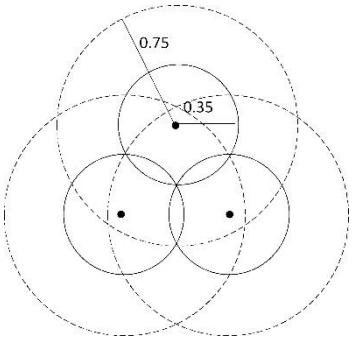
(a) Rectangular cell distribution with low fill factor



(b) Rectangular cell distribution with high fill factor



(c) Triangular cell distribution with low fill factor



(d) Triangular cell distribution with high fill factor

Figure 19 - Studied cell distributions. The cell distributions have been divided respect to its geometry and fill factor.

It can be observed in the summarizing table 9 that the best option given the current restrictions and assumptions is the triangular cell distribution with high fill factor. It is straightforward to demonstrate that is the distribution that minimizes the overlaps. The covered area shown in Table 9 takes into account that only 6 transmitters are available.

Distribution	Covered Area	Fill factor	Separation
Rectangular low fill factor	2.3 m^2	68 %	70 cm
Rectangular high fill factor	1.88 m^2	100 %	50 cm
Triangular low fill factor	2.3 m^2	78 %	70 cm
Triangular high fill factor	2 m^2	100 %	60 cm

Table 9 - Summary table of the analysed cell distributions

The next actions will be:

- Analyse the SINR probability density function
- Define, the best handover strategy taking into account the current results
- Analyse several random walks
- Obtain the optimal transmitter (multi-emitter), receiver (multi) and cell distribution characteristics attending to be defined with optimisation criterion (SINR PDF, covered area, etc…).

2.3.5 Thermic Consideration for Compound Parabolic Concentrators

When concentrating light into a photodiode, the thermodynamical maximum ratio of concentration C_{max} permits to relate the angular acceptance and a constant energy distribution onto the PD [8], [9]. For a source located at infinity this ratio is

$$C_{max} = \frac{n_{cpc}^2}{sin^2\left(1/2\, FOA\right)}.$$

Subindex cpc states for compound parabolic concentrator and n is the refractive index; FOA is for Field of Acceptance. As an example, for plastic material like polycarbonate PC with a refractive index of 1,555 at a wavelength of 860 nm and FOA=30°, C_{max} is 36. With this result, the maximum CPC aperture can be calculated as follows

$$C_{max} = \frac{d_{ap}^2}{d_{PD}^2},$$

Where d_{ap} is the aperture diameter and d_{PD} the diameter of the photodiode. Taking a PD = 3 mm, d_{ap}=18 mm, and d_{ap}=11,7 for a PD=1,95 mm.

3 Wireless transmission

3.1 Radio link

3.1.1 Main objectives

The main wireless radio transmission objective of this project is to propose innovative radio interface that allows the system to achieve high data throughput. Some innovative solutions will be used to achieve these objectives. First, the design of an RF radio front-end at 240 GHz is explored to be able to transmit with high frequency bandwidth as well as digital signal processing techniques such as advanced channel (de)coding scheme at high throughput, use of multi-antenna array for spatial stream multiplexing.
This radio link section will propose some issues in order to achieve real time hardware implementation for virtual reality transmission. These proposals are linked to the hardware implementation feasibility in terms of components and platforms.
The first objective is to specify the first components that will be implemented for the V1 demonstrator based on 60 GHz RF front-end with at least 4 or 5 Gbps data rate transmission per user.
The second demonstrator will integrate a 240 GHz RF front-end and a throughput of at least 10 Gbps per user is targeted.

3.1.2 RF Front-end

In order to utilize the wide bandwidth available in the sub THz range (e.g. 240 GHz), innovative circuit and system techniques need to be implemented. Thanks to the continuous enhancement in the silicon technologies, integrated circuits and systems at such high frequency are possible with high level of integration because of the small form factors at such frequencies.
Although the huge potential, there are many challenges as well. The limited available output power at such high frequencies and high achievable minimum noise figures leads to a very strict link budget analysis (see 3.1.4.1). In addition, the transistor model accuracy is an issue that to be included as well as the sensitivity of the measurement setups. These challenges and other are to be addressed during the design activity in WORTECS project.
A typical IQ analog front-end shown in Figure 20 consists of a transmitter which is up-converting the baseband I and Q signals directly to the RF frequency where they are added to generate the IQ signal. This signal is further amplified and transmitted through an antenna. The signal is then received at the receiver side and down converter with an IQ mixer. As can be seen in Figure 20 a main building block is the generation of the LO frequency with enough power and bandwidth to drive the fundamental mixer.

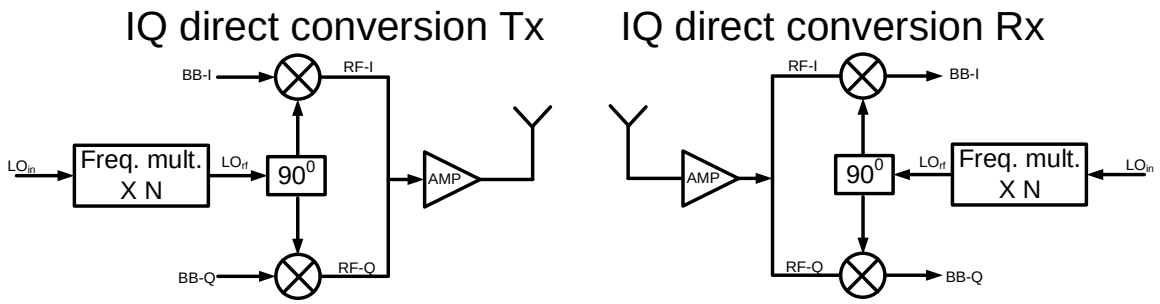


Figure 20 - IQ front-end

RF Carrier generation

The first step would be to generate the 240 GHz local oscillator signal for the up converting and down converting mixers. This was performed in the literature with several architectures, by using a fundamental oscillator at high frequency which saves power but limits the achievable phase noise due to the degraded quality factor of the passives at such a high frequency. Another solution is to use injection locked oscillators which is still a power efficient architecture but might be limited in the locking range or also to use a multiplication chain that multiplies a low frequency signal by some multiplication factor to generate the sub-THz signal. Although the later approach is more power consuming it allows for broadband LO bandwidth which is beneficial in multi-channel application scenarios.

For that reason in this project the later choice to generate the LO frequency is to be followed. The frequency multiplier chain generates the required fundamental frequency and some unwanted harmonics at a spacing of Lo_{in} from the fundamental tone. For that reason the choice of the input frequency (LO_{in}) and so the multiplication factor (N) depends on the baseband channel bandwidth, so that it is guaranteed that the unwanted harmonics will not generate unwanted image signals on top of the desired signal. For a baseband channel bandwidth of 10-15 GHz the LO_{in} should be 20-30 GHz, and then a multiplier by 8 chains is needed to generate the 240 GHz LO signal as shown in Figure 21, where a quadrupler is used to generate the 120 GHz signal which is then amplified and then multiplied by 2 to generate the 240 GHz signal.

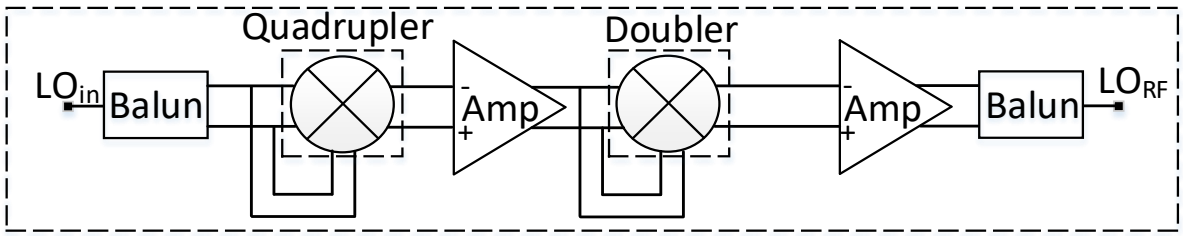


Figure 21 - LO multiplication chain (Freq. Mult. XN)

Multiple elements array

Due to the strict link budget, beam forming is to be utilized as a solution to focus the beam and enhance the achievable communication ranges. Different phased array systems were presented in the literature: RF beam forming, LO beamforming and baseband beamforming.

Comparing the RF beam forming and LO beamforming

The LO beam forming although has less cascaded stages in the RF signal path as shown in Figure 22 compared to structure shown in Figure 23 but consumes more power due to the replication of the RF mixer and frequency multiplications chain.

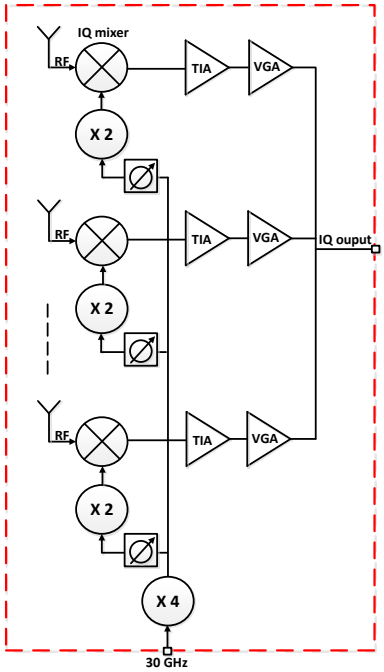


Figure 22 - LO beam forming architecture

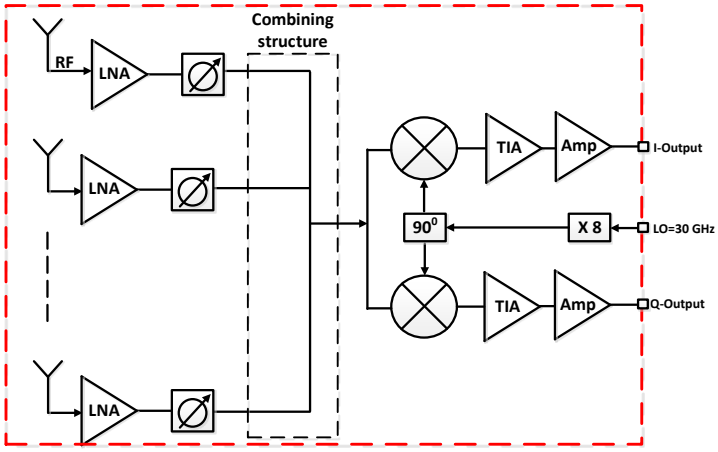


Figure 23 - RF beam forming architecture

The topology of the vector modulator, depending on the phase resolution, can be realized using two VGA fed by IQ signals and added to control the vector magnitude and gain as shown in Figure 24. Additional care should be given for the phase variation of the VGA across the frequency to reduce the beam squinting.

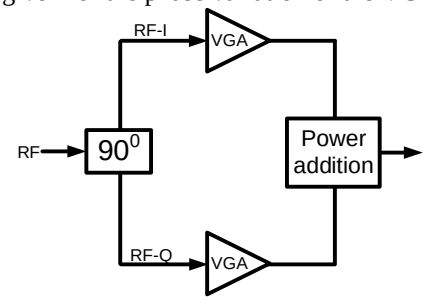


Figure 24 - Vector modulator architecture

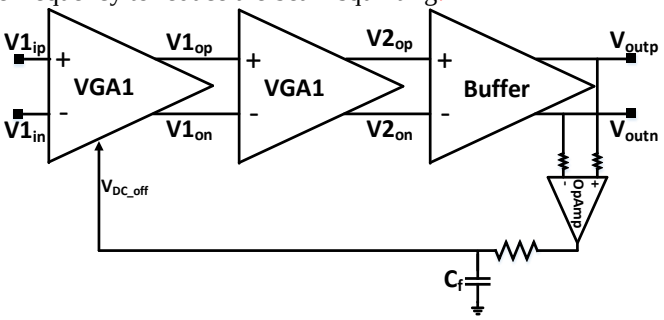


Figure 25 - Rx baseband chain

Some circuit idea's for enhanced performance

At the receiver side, in order to enhance the achievable bandwidth and conversion gain, a trans-impedance amplifier, as shown in Figure 22 and Figure 23, is proposed as a load for the mixer, which decorrelates the gain-bandwidth trade-off, experienced when designing the conventional Gilbert cell mixer with resistive load. In order to realize a practical system the direct conversion receiver is to be equipped with VGA chain and DC offset cancellation loops, as shown in Figure 25, where the output DC voltage is sensed and compared through a differential operational amplifier to generate an error signal that compensate for the output DC offset within the first VGA. This eliminates the need to use bulky series DC blocking capacitors and allows for lower low-cut-off frequency for the receiver.

3.1.3 Digital front end – Baseband processing

As mentioned previously in section 1.2, low latency compressed video bandwidths of 13.6 and 120 Gbps per user are expected for high resolution, high refresh rate HMDs. Achieving these bandwidths is almost impossible with the current solutions commercially available for the 2.4/5 and 60 GHz bands. The new IEEE 802.11ax standard introduces a modulation coding scheme (MCS) for achieving a data rates of approx. 10 Gbps in the 2.4/5 GHz band by using a channel bandwidth of 160 MHz and a 8x8 MIMO (8 spatial streams). Nevertheless, this would be rarely possible, due to the crowding of the 2.4/5 GHz bands. In rare cases, when these data rates can be reached, due to the path loss, they would be available just a few meters around the access points [ref]. This would still not satisfy the needs for achieving 13.6/120 Gbps per user, needed for the VR use case.

In WORTECS we are aiming at overcoming this main issue, i.e. achieving the needed throughput. Achieving them in the current 2.4/5 GHz ISM bands is impossible for the proposed use cases, especially for the VR use

case. The main reason is the available link budget, limited by the allowed transmit power and the usable distances. In order to increase the available channel capacity, a common approach is to use higher channel bandwidths, when the transmit power is constrained.
The digital front end, i.e. baseband processing, should support high data rates and low latency in order to satisfy the requirements for the most demanding VR use case. In WORTECS the baseband processing would be developed in two steps. This is needed because the 240 GHz AFEs are not yet available and therefore it was decided to use available 60 GHz AFEs from IHP and/or commercial ones from Infineon, Analog devices or SiversIMA to validate the VR transmission with the digital baseband processing. However, the channel at 240 GHz and 60 GHz would differ and, therefore, tuning of the parameters of the baseband processor would be needed.
In the 60 GHz channel, a bandwidth of 2 GHz per channel is available. Nevertheless, only 1.7 GHz are used, in order to avoid inter-channel interference (ICI). There are a total of 4 channels. In Table 10 the channel capacity for different SNRs is calculated.

SNR [dB]	0	5	10	15	20	25
Channel capacity [Gbps]	2	4.11	6.92	10.06	13.32	16.62

Table 10 - Channel capacity of 2GHz channel

As can be seen, the 2 GHz channels have a maximal capacity of 16.62 Gbps for SNR equals to 25 dBs. If the channel bandwidth is reduced to 1.7 GHz the capacity would be also reduced. Therefore, only the required data rates of 13.6 Gbps can be achieved per channel. Nevertheless, due to implementation constraints achieving the channel capacity is also an issue. Therefore, much lower data rates would be expected (4-5 Gbps) with the currently available hardware for the first demonstrator.
We choose an OFDM system for the first demonstrator. The main reason is that the channel equalization is much simpler when OFDM is used compared to a single carrier modulation. In the 60 GHz band, the antenna gains must not be so high, since the free space loss is much lower compared to that at 240 GHz. The lower antenna gain implies a broader radiation pattern, which on the other hand leads to a larger number of multipath components arriving at the receiver. Anyway, broader radiation pattern means that the use of beamforming/ beamsteering antennas will not be in the first demonstrator version.
The architecture of the 60 GHz transmitter is shown in Figure 26.

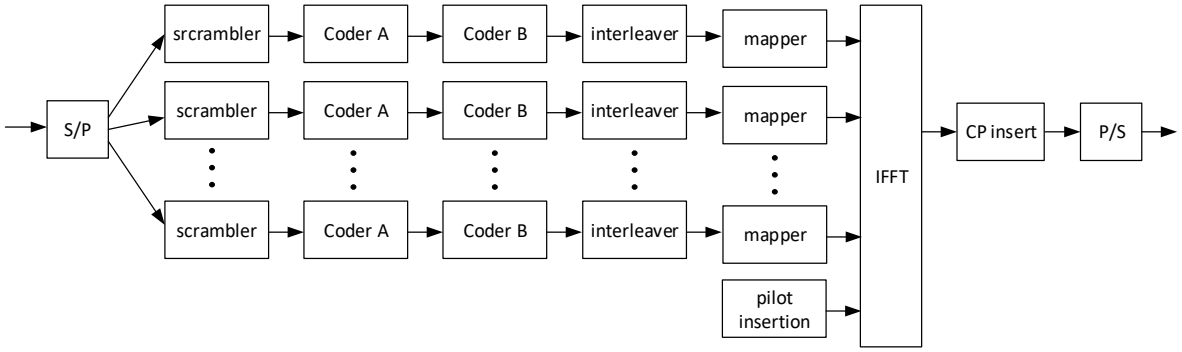


Figure 26 - Block diagram of a paralelized OFDM transmitter

It can be noticed in Figure 26 that the most of the operations performed in the transmitter are parallelized. This parallelization is needed for high data rates since the digital hardware is not capable of processing such a high throughput data streams. The architecture is standard, with outer and inner channel code. The choice of codes would be described later in this section. The interleaver is used to avoid burst errors and the scrambler is used to randomize the incoming data stream. There are standard architectures which can be used for the both scrambler and the interleaver [ref]. After mapping incoming bits to symbols in a given modulation scheme, an IFFT is performed and the signal in time domain is obtained. A cyclic prefix is inserted to avoid inter-symbol interference due to the multipath propagation channel, and the signal is converted to a serial stream, ready to be sent to a digital to analog converter. The number of points in the IFFT is basically dependent on the channel coherence bandwidth. Usually, 512 or 1024 point IFFT is significant for the 2 GHz channel in the 60 GHz band [ref].

The architecture of the receiver data path is given in Figure 27

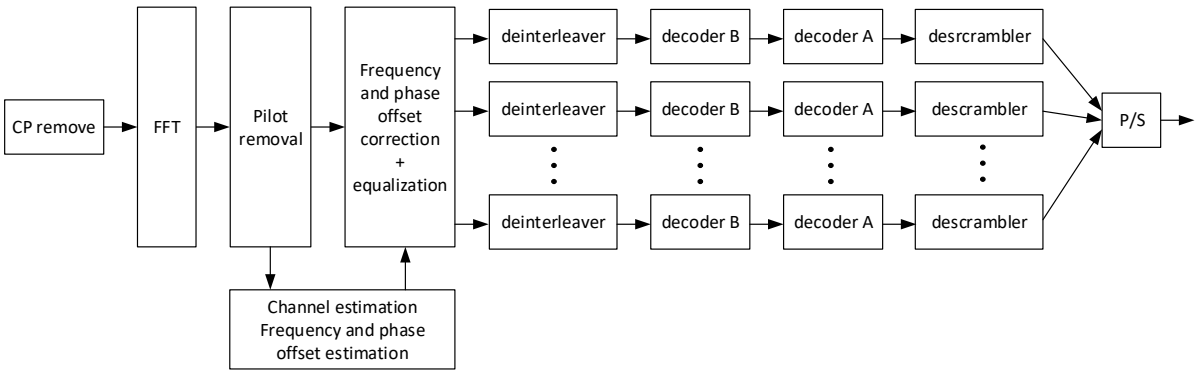


Figure 27 - Parallelized OFDM transmitter

After removing the cyclic prefix and performing FFT, the pilots are removed and the channel is estimated for time and frequency synchronization, and equalization processing.
Before processing the incoming frames, the frame arrival should be detected using a synchronizer. This synchronizer can be 802.11ad like, or if the available FPGA resources are limited a simpler synchronizer can be deployed. This is possible, since the expected interference in 60 GHz and especially 240 GHz bands should be minimal due to the beam-steering high gain antennas that should be used.
In order to achieve higher throughputs in the 240 GHz band, additional optimization of the baseband processor should be performed. Since in the 240 GHz band, high antenna gains should be used in order to increase the link budget, sparse to none multipath propagation is expected and OFDM might not be needed. The large bandwidths available (> 20 GHz) allows high signalling speeds, which on the other hand allows the use of simpler modulation coding schemes. These are single carrier schemes which include BPSK, OOK [ref].These modulation schemes can be used to achieve throughput higher than 10 Gbps.
Parallelization of the most of the tasks performed in the baseband processor should enable high throughput and low latency. Initial tests performed show that a throughput of 4 Gbps in the 2 GHz channel is possible. Also, the latency can be reduced down to 100 microseconds if convolutional codes with Viterbi decoders are used.
The baseband processor should also support ranging and localization. Due to the large bandwidths available, a sub-centimetre ranging/localization precision/accuracy should be achievable.

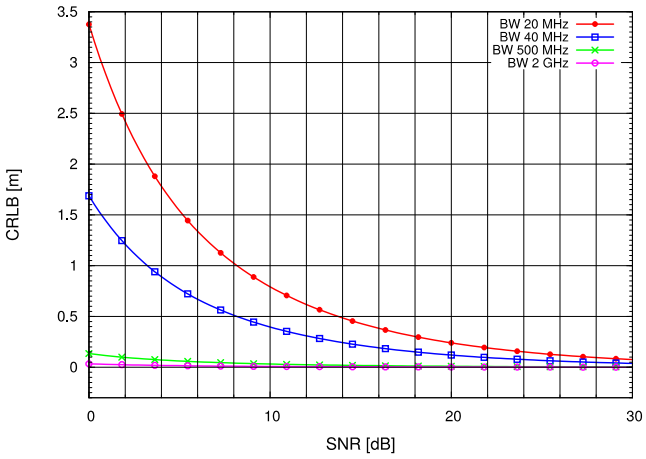


Figure 28 - Cramer-Rao lower bound for ranging

In Figure 28, the Cramer-Rao lower bound for ranging is shown. This bound gives the achievable ranging precision for a given SNR regarding to the channel bandwidth. Higher the channel bandwidth is, more accurate the ranging is. In Figure 28, the time-bandwidth product of the signal is 1. As can be noticed, for bandwidths of 2 GHz the ranging precision is in the centimeter level.

3.1.3.1 FEC Coding Schemes

Error correction coding is used to ensure that the information received is correct and has not been corrupted due to the noisy wireless channel during transmission. FEC is an error correction scheme usually realized by adding redundant data to the transmitted data in order recover the original data in the receiver. When using FEC, the receiver does not require from the sender to retransmit the data.

FEC codes can be classified into two classes; convolutional codes and block codes. Block codes are processed block by block basis while convolutional codes are processed on a bit by bit basis. Classical block codes such as Reed-Solomon are usually decoded using hard-decision decoding. In contrast, convolutional codes are typically decoded using soft-decision algorithms such as the Viterbi or BCJR algorithms and allow for much higher error correction performance than hard-decision decoding but at the expense of exponentially increasing complexity.
Modern FEC codes include Low-Density Parity-Check (LDPC), turbo, and polar codes. LDPC codes are adopted in many standards for example, Wi-Fi (802.11n, .11ad, 5G NR) and DVB-S2 standard for the satellite communications. There are also some practical applications for turbo codes such as HSPA, LTE, and WiMAX. Polar codes are gaining much attention in the recent years since they are used in 5G NR specification for controlled signals.

1. Low-Density Parity Check (LDPC)

   LDPC codes are a class of linear block code. The term "Low-Density" refers to the characteristic of the parity check matrix which contains only a few "1"s in comparison to "0"s.
   Parameters: code length n, with k information bits, and an $m \times n$ parity-check matrix H.
   An (n, k) block code takes k bits at a time and produces n bits and the code rate $R=k/n$.

   - Possible parallel implementation of the decoder which leads to higher throughput
   - For a given spectral efficiency, the LDPC code outperforms the RS code by roughly 3 dB (IEEE 802.3bn)
   - Decoders: sum product algorithm (SP), belief-propagation (BP) decoding and bit flipping algorithm
   - Disadvantage: error floor; conventionally the BER steadily decreases in the form of a curve as the SNR increases. Error floor is a point after which the curve does not fall as quickly as before
   - Implementation example: a decoded throughput (T/P)= 78 Gbps and a latency of 0.06 μs have been demonstrated in [10] for an LDPC code having a block length of K = 1723 and a coding rate of R = 0.84

2. Turbo

   It is the concatenation of two convolutional codes separated by an interleaver. Hence, it can be concatenated either in serial, parallel or hybrid manner.

   - Decoders: max-log approximation and soft-input soft-output (SISO) decoding
   - Disadvantages: higher latency than the LDPC code due to usage of interleaver and it also suffers from error floor
   - Implementation example: authors in [11] demonstrated a fully-parallel turbo decoder that achieves a decoded throughput of 21.9 Gbps and a processing latency of 0.24 μs, for a turbo code having a block length of K = 6144 and a coding rate of R= 1/3

3. Polar

   Polar codes are currently under consideration for potential adoption in future 5G standards. They are constructed as a result of the channel polarization transform.

   - They have a very low error-floor
   - Decoders: successive-cancellation (SC) decoding, successive cancellation list (SCL) decoding, and belief-propagation (BP) decoding
   - Disadvantages: polar codes are not universal due to dependency on the underlying channel. If a channel is unknown to a transceiver, erroneous decoding can occur. Polar decoders are in serial nature leading to lower throughput compared to other schemes

In general, different FEC schemes can have significant differences in decoding performance, processing latency, and area requirements. Hence, an optimum FEC scheme is desired to well satisfy the requirements of the target application. To decide which FEC scheme is the best fit to the requirements of use-cases in WORTECS, the following performance metrics are taken into consideration.

1. Bit Error Rate performance (BER)
2. Throughput
3. Latency
4. HW Efficiency

A recent work published in [12] sets a comparison between the coding schemes in terms of the BER of different information block lengths (*K*), and code rates (*R*). The authors applied using Binary Phase Shift Keying (BPSK) modulation over the Additive White Gaussian Noise (AWGN) channel. They chose LTE implementation for convolutional and turbo codes. For LDPC, they used the IEEE 802.16 codes, while using the Bhattacharya bounds algorithm to construct polar codes. The turbo decoder consists of two SISO decoders. Decoding of LDPC codes is performed with the SP Algorithm. The polar code decoding is handled by the standard SC algorithm. Some performance results can be shown in Appendix A.
Authors in [13] provided a comparison of hardware efficiency between polar, turbo and LDPC decoders in terms of area and time complexity of ASIC implementations. Here, the IEEE 802.11ad standard uses Quasi-Cyclic LDPC (QC-LDPC) codes with a block length of $K = 672$ and code rates $R = \{1/2, 5/8, 3/4, 13/16\}$. The authors simulated the performance of the IEEE 802.11ad LDPC code using a layered offset min-sum decoding algorithm. These metrics were plotted against each other on a double-logarithmic plot where the area and time complexity are on the vertical and horizontal axes, respectively. The hardware efficiency is defined as unit area per decoded bit and is measured in mm^2/bits/s. In addition, decoding throughput is the inverse of decoding time and denoted as T/P. Some metrics are also given in Appendix A.

Table 11 summarizes the performance of the main decoding schemes.

FEC Scheme	**Metric**			
	BER	Throughput	Latency	HW Efficiency
LDPC	Similar	High	Low	High
Turb1	Similar	High	Moderate	Moderate
Polar	Similar	High	High	Moderate

Table 11 - Hardware efficiency of 3GPP LTE decoders

3.1.4 Performance evaluation

3.1.4.1 Link budget

This sub-section covers link budget calculations for the radio wireless link. The final demonstrator will operate at the carrier frequency of 240 GHz which has been covered in part a). For the purpose of V1 demonstration, a 60 GHz design will be used. The corresponding radio link calculations are presented in part b).

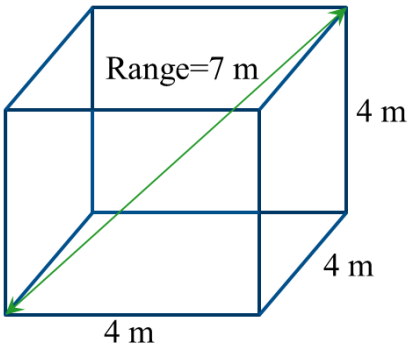


Figure 29 - Multigigabit model block diagram

Part a) 240 GHz radio

Room of size 4m x 4m has been envisaged for the VR use case. We assume the room height to be 4 m. The user can move anywhere in the room with an indicative speed of 4 km/h. So, the radio link should cater for the range of 6.93 m which the length of the largest diagonal in the room. Free space path loss (FSPL) for a radio link is given by FSPL (in dB) = 32.45 + 20 $\log_{10}$ (frequency in MHz) + 20 $\log_{10}$ (distance in km). For a range of 7 m, FSPL is about 97 dB.
Based on measured values, the RF signal level at the transmitter output is 0 dBm. Return loss is about 7 dB and better across the 10 GHz bandwidth of operation. Mismatch loss due to S11 of -7 dB is about 1 dB i.e. with output signal power of 0 dBm from the transmitter, -1 dBm signal power actually enters into the antenna. Based

on HFSS simulations, the antenna efficiency is 50 % and better i.e. there is a 3 dB loss within the antenna. So, -4 dBm of signal power is radiated out of the antenna. Based on current measurements, antenna gain is 5 dBi. So, the effective isotropic radiated power (EIRP) turns out to be 1 dBm.
For a bandwidth of 10 GHz, the thermal noise power is -74 dBm. Receiver noise figure is expected to be better than 15 dB. This leads to noise floor of -59 dBm. With EIRP and FSPL of 1 dBm and 97 dB respectively, the signal power level of -95 dBm (approximate) is expected at the receiver, with reciprocity assumed for the receiver antenna.
Thus, the signal-to-noise ratio (SNR) of -36 dB is expected at the receiver in the worst case with the user being in the diagonally opposite corner with respect to the transmitter location in one of the top corners of the room. With the user being in the centroid of the floor, the range is about 4.8 m for which the SNR is about -32.5 dB.

Part b) 60 GHz radio

It is planned to use a 60 GHz radio at IHP for V1 demonstration. The unlicensed 60 GHz band spans from 57 to 66 GHz. Four channels with equal width of 2.16 GHz are defined. Channels 1, 2, 3 and 4 have carrier frequencies 58.32, 60.48, 62.64 and 64.80 GHz, respectively. For channel 3, the transmitter output power is 0 dBm. VSWR is better than 2:1 amounting to 0.5 dB mismatch loss. Antenna efficiency is typically 75 % which is equivalent to -1.25 dB loss. Measured antenna gain is about 17 dBi. So, the EIRP is 15.25 dBm. As the carrier frequency is about a quarter of 240 GHz, FSPL decreases by 12 dB. The FSPL for 60 GHz link at a range of 7 m, is about 85 dB.

Occupied channel bandwidth of 1.76 GHz will be used to demonstrate live video communication over 60 GHz link for V1 milestone. For 1.76 GHz, the thermal noise power is about -81.52 dBm. Typical noise figure for 60 GHz receivers is about 7 dB. So, the noise floor is -74.52 dBm.

15.25 dBm EIRP and 85 dB FSPL yield signal level of -54.5 dBm at the receiver, with reciprocity applied for the receiver antenna. This yields SNR of 20 dB for channel 3. The SNR for channel 4 is almost equal within +/- 1 dB. Channels 1 and 2 will have about 10 dB lower SNRs due to reduced EIRP on account of lower gains from the transmitter amplifiers and variations in FSPL, VSWR, beam squints, etc. over frequency.

3.1.4.2 Overall latency

The main latency of the system depends on the interleaver, FFT/IFFT in OFDM system the channel equilizer and the channel coding/decoding. The latency of the interleaver can be controlled by its length. FFT/IFFT can be also implemented in quite efficient way. Having a larger radix FFT/IFFT reduces the latency. The main latency comes from the FEC coding/decoding.

3.1.5 High throughput LDPC for WORTECS use case

The LDPC code offers a simplification of the channel coding requirements. Indeed, in contrast with Turbo or convolutional code, LDPC does not need interleaving function to increase the BER performance if the channel is not a AWGN one. Furthermore, the puncturing, selected in many standards to settle a good spectral efficiency / throughput compromise, is avoided with the selection of a typical set of LDPC codes.
At the transmission part, the LDPC coding shall respect the specification of the codes. The architecture is the only consideration point to target a high throughput and competitive hardware architecture.
At the reception part, the LDPC decoding key axis shall discuss on a compromise between Bit Error Rate, latency, HW efficiency and throughput. LDPC codes benefit from iterative decoding algorithm. An extensive number of iterations increases the BER, but also the latency, the HW efficiency and/or the throughput. The number of non-null elements impacts the number of operations. The LDPC protograph specifies the transfer of updated message.
The next section proposes a first architecture for a LDPC coder and a LDPC decoder, to compare and select a specific LDPC code. This architecture has been designed to target a large variety of QC-LDPC codes. It is not optimized to reach WORTECS objectives. A second highly pipelined architecture, focused on one typical code, will increase the throughput and optimize the hardware efficiency.

3.1.5.1 LDPC Transmission part

The LDPC coding consists in the resolution of equation $H.c^T = 0$, where c^T is the sent code word. The coding part is focused on QC-LDPC codes, where the matrix H is represented through circular identity or null $z \times z$ matrices. In practice, $H = [H_1 \quad H_2]$ such as the parity calculation consists in inverting the matrix H_2. Double-diagonal QC-LDPC matrices is a typical form of the matrix H_2, shown in Figure 30 and selected in IEEE 802.11n/ac, 802.16 or 5G NR. It offers a realistic coding architecture with a native parallelism depending on the expansion factor z.

9	117	204	26	-	-	189	-	-	205	0	0	-	-
167	-	-	166	253	125	226	156	224	252	-	0	0	-
81	114	-	44	52	-	-	-	240	-	1	-	0	0
-	8	58	-	158	104	209	54	18	128	0	-	-	0

Figure 30 - Double Diagonal QC-LDPC representation (from 5G NR, BG2, z=256)

3.1.5.2 LDPC Reception part

The reception part shall address the soft bit information or Log Likelihood Ratio (noted LLR) extracted from the received mapped symbols. The LLR links the probability that the bit is equal to 0 and that it is equal to 1, according to the formula:

$$LLR(b) = log\left(\frac{pr(b = 0|x)}{pr(b = 1|x)}\right)$$

In this formula:

- x is the complex symbol of the IQ diagram
- b is a bit mapped on the complex symbol

The LLR is represented on a signed value, with 8 bits quantization. The decoder follows the Horizontal Layered Belief Propagation algorithm.

3.1.5.3 Interfaces

This block is coded in VHDL and is compiled with either Intel (Formerly Altera) or Xilinx tools. The FEC uses only one master clock. It benefits from versatile data interfaces which are compatible with Intel Avalon streaming or ARM AXI4 streaming buses.

The LDPC encoder processes $k = z.k'$ bits and extracts $n = z.n'$. The LDPC decoder processes $n = z.n'$ soft bits and returns $k = z.k'$ hard decision. Due to the native parallelism of the QC-LDPC codes, blocks of z bits feeds and are extracted from the modules per clock cycle. Figure 31 shows a typical chronogram associated to the design.

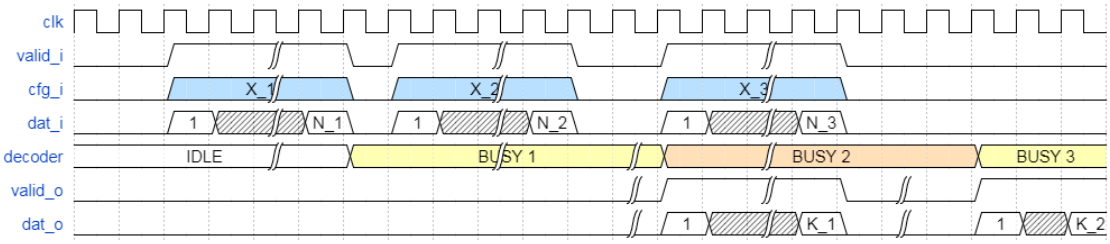


Figure 31 - Receiver chronogram

3.1.5.4 Hardware performances

Figure 32 gives the radio and the useful throughput reached at 200 MHz for the encoder (a) and the decoder (b) module. The maximal expansion factor is $z = 32$. The figures show higher throughput for high rate codes.

Figure 32 - Transmission and reception throughput estimation

Table 12 underlines the equivalent required hardware resources. Each chip runs at 200 MHz clock speed. These figures lead to a trend to define a typical code. An optimized architecture shall target the WORTECS objectives.

	Resource	**Transmission**	**Reception**
Virtex 6	*Slice Registers*	1632	28162
	LUTs	4083	65493
	LUT Flip Flop	4994	65461
	BRAM	2	241
	DSP48E1	1	2
Arria 10	*Logic utilization (ALMs needed)*	24710	40237
	Combinational ALUT usage for logic	15250	57000
	Dedicated logic registers	34584	28461
	Total block memory bits	78848	349
	Total DSP Blocks	1	2

Table 12 - Resource estimation for Xilinx Virtex 6 and Intel Arria10 FPGA chips

3.1.5.5 Optimization opportunities

The architecture described in this section fits with any LDPC codes and shares the computing resources.
A future version, planned to run at 250 MHz, will encode on the fly the data stream and avoid the data buffering. By this way, one instance with a LDPC coding rate $\frac{5}{6}$ and $z = 64$ shall provide more than 10 Gbps data stream.

The current LDPC decoder shares the computing resource between layer update and iteration. With some duplication, the future version shall upgrade considerably the throughput. The throughput will then not suffer from the number of iterations. Furthermore, by rearranging the decoding operations, the future version will avoid several waiting cycles, and so be more efficient in term of throughput and latency. With 250 MHz clock speed and no waiting cycles, a LDPC code with rate $\frac{5}{6}$ and $z = 64$ shall provide more than 15 Gbps useful throughput.

3.1.6 HW specifications

From the RF front end point of view

The antenna is intended to be integrated on chip in order to guarantee a stable and reproducible performance. While the interface of the LO signal at 30 GHz is intended to be single ended to simplify the board routings especially if multiple chips are to be used on the same board. The baseband interfaces are intended to be differential.

The board is required to be a high frequency board in order to carry the high frequency LO signal and the broadband baseband signals. While the connectors to be used are under investigation to guarantee that the connector-board interface will not limit the achievable bandwidth.

The digital part of the radio should be implemented on an FPGA boards. This is needed due to the available flexibility as well as the performance the new generation FPGA devices can offer. The FPGA itself does not have data converters and, therefore, additional analog-to-digital and digital-to-analog converters must be used.

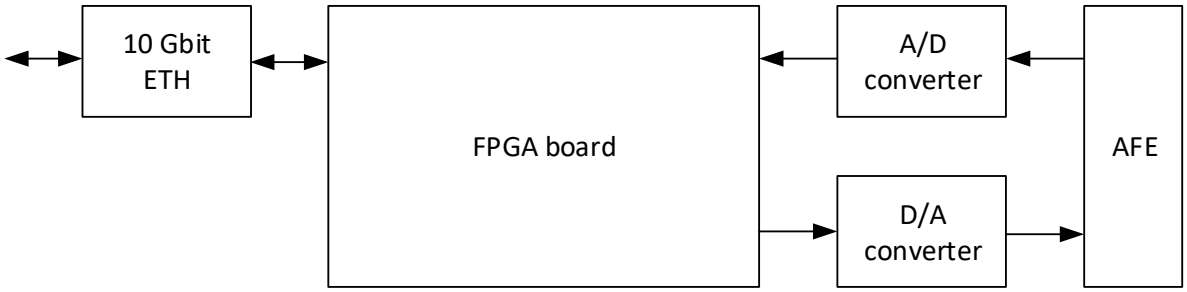


Figure 33 - Multigigabit modem block diagram

In Figure 33, a block diagram of a multigigabit modem is given. The data converters are connected to the FPGA board using standard digital interfaces (serial or parallel). The anlog front-end has analog inputs and outputs for the baseband signal which are connected to the data converters.

The FPGA board to be used is a board developed at IHP and known as digiBackBoard.

Figure 34 - digiBackBoard

This board has a ZYNQ7045 SoC and can be upgraded with ZYNQ7100 if more FGPA resources are needed. The A/D and D/A converters support 2.16 GSps per I and per Q signals. The board has 4x 1 Gbit ETH ports and also has extension connectors where an adapter board with 10 Gbit ETH can be attached.

Connecting this board to the MAC would be performed using the 10 Gbit ETH interfaces, while the connection to the AFE would be performed using coax cables. The signal can be differential or single ended.

Additionally, as a backup solution, another commercial FPGA board can be considered. A board which can be used is, for example, VC709 from Xilinx which has an FMC connector onto which an A/D-D/A converter boards can be attached. This FPGA board does also have 4 SFP+ cages, which can be used for 10 Gbit Ethernet.

Additionally a A/D and D/A cards can be attached to the FMC port. Such a card is shown in Figure 35.

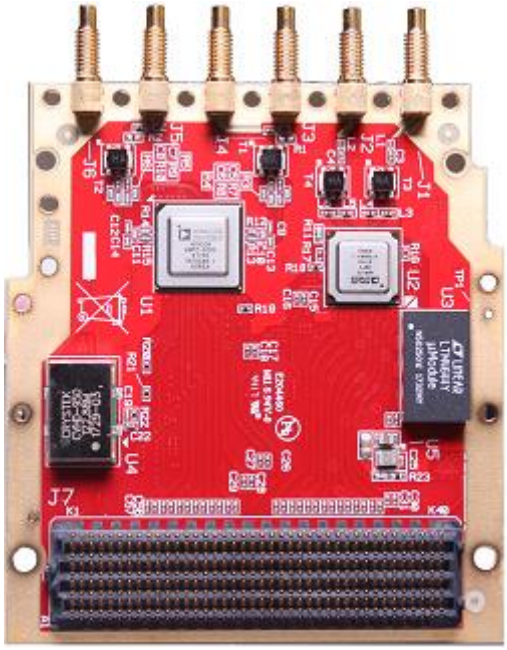


Figure 35 - A/D and D/A on a single FMC card

3.1.7 Potential risks

From the RF components point of view there are several risks

1- The accuracy of the models compared to the measured data might be crucial especially for the vector modulator calibration scheme, because the phase at such high frequencies is not easily modelled.
2- The output power is limited at such high frequencies, and so to achieve the required output power and, therefore, the required communication range while maintaining reasonable thermal performance is a challenge.
3- In order to enhance the link budget multiple chips might be needed to be integrated on the same chip, this is a challenge and need to be studied carefully before hand to design the chips fitting this criteria.
4- The on-chip antenna's has low form factor, but for antenna array a λ/2 spacing need to be kept, which consumes a lot of on chip area, so the utilization of this area is also a challenge adding to it the antenna array design by itself.

At this phase, multiple risks can be detected regarding the baseband design. First of all are the risks associated with the first demo which has to work at 60 GHz. The main risk is that the overall system cannot achieve data rates larger than 1 Gbps, due to the high noise levels. The chances for this are quite low since the analog frontends were already tested with an AWG and a scope. The tests show that data rates of up to 4 Gbps are possible with these analog frontends. It might happen that the A/D and D/A converters introduce additional noise and further reduce the link budget, which would at the end affect the final data rate which can be achieved.
For the second demo at 240 GHz, the link budget calculations show that significant gain is missing. This can be solved in a few different ways. First, antennas with high gains can be used. This solution should be additionally tested. Second, higher output power can be transmitted. This can be solved by using antenna arrays with multiple elements, each element being supplied by a separate power amplifier. Nevertheless, if this approaches fail, it would be hard to reach multi gigabit data rates for distances envisioned in this project.

3.2 Optical link

3.2.1 Main objectives

The main objective is to define the main components for achieving a high throughput optical transmission dedicated to VR demonstration. Two demonstrators are planned to be implemented during the project's life increased evolutions.

Demonstration 1:
This focuses on a high density network that can provide > 1 Gbps per user (full duplex) with multi user, but has the potential to provide Tbps per room, or coverage 'space'. This will be achieved using Optical Wireless Communications. The OWC systems will provide bandwidth density and user data rates beyond what is available in commercial systems today (~40Mbps), again showing substantial increases up to several Gbps on point to multipoint configuration. Virtual Reality is targeted as a demanding application. The system will be linked to the BCOM setup and connected to a server in order to provide the Virtual Reality content to head mounted display terminals.

Demonstration 2:
This focuses on ultra-high data rate links. The WORTECS project will use, in this second phase, a novel fibre-wireless-fibre (FWF) approach to create point-to-multipoint Tbps capable links. Additionally, this will lead to cm precision positioning data for terminals.

3.2.2 Optical Wireless Communications PoC v1

3.2.2.1 Pre-prototype with Power Line Communication (PLC) device

System Overview:
We have begun investigations by developing an easy to integrate, compact and cost effective OWC demonstrator, while relaxing the data-rate targets. Our work is based on ACEMIND European collaborative project [14] where we wanted to associate two technologies, Visible Light Communication (VLC) and Power Line Communication (PLC) in order to optimize both infrastructure network and Access Point (AP).
The concept was already introduced [15], whereas the one of the goals of the current project is to take advantage from latest PLC (Power Line Communication) innovations and apply them in the OWC. Indeed, conventional PLC products use two of the three copper wires (Phase P and Neutral N) to provide power-line Internet. The latest standard HPAV2 offers the possibility to access in addition to Ground G conductor and exploit the physical potential of this electric cable with additional features such as: Time Division Duplexing (TDD) mechanism, MIMO (Multiple Input Multiple Output) capability, OFDM (Orthogonal Frequency Division Multiplexing) modulation and Turbo Convolutional Code (TCC) higher Code Rates (8/9 code rate).
The result is not only significantly a better performance for transmissions, up to 1300 Mbps, but also higher range. Our innovation is based on the use of these dual channels in PLC field by the use of two distinct wavelengths in the OWC domain. The additional novelty is to perform the data detection at the receiver side in a differential mode, as already shown in work [16] and thus increase link performance including throughput and distance in OWC domain.

Figure 36 a) shows the conventional HPAV2 MIMO communication principle with "tp-link" selected PLC plug, AV 1300 Gigabit.

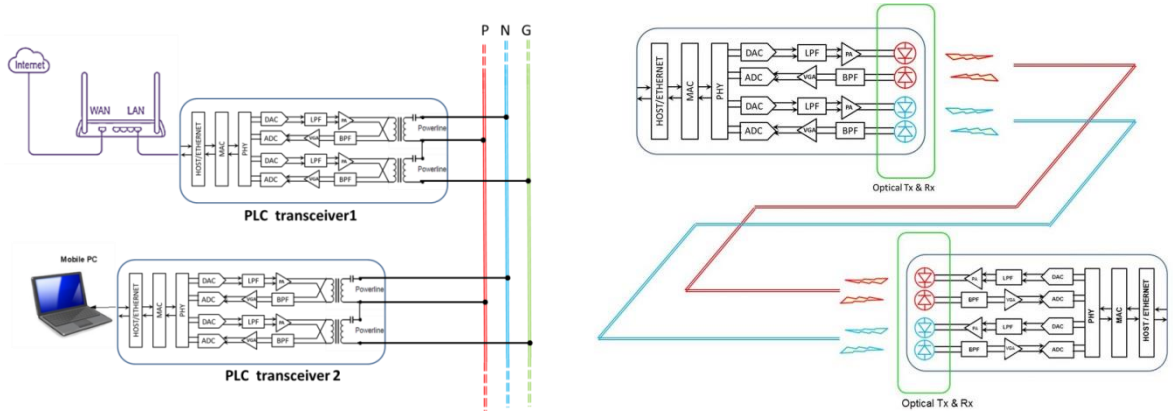


Figure 36 - a) PLC kit "tp-link"-AV1300 Gigabit and b) PLC link with optical wireless communication adaptation

Figure 36 b) shows the modifications achieved to obtain OWC link from two devices. The electrical power-coupling module has been removed and replaced by, for each Plug, the following elements. On emitter, we mount Light Emitting Diode (LED) infrared emitter (850 nm) – SFH 4557 from Osram and LED infrared emitter (950 nm) – SFH 4547 from Osram with Current Amplifier for each LED. On receiver, we assemble Polymethylmethacrylate (PMMA) Hemispherical lenses with 10mm diameter associated to an optical bandpass filter with +/- 25 nanometer (nm) around the central wavelength (850 and 950 respectively); then Positive-Intrinsic-Negative Photodiode (PIN PD) – SFH 2500 from Osram with 800/1000 nm range linked to Complementary Metal-Oxide Semiconductor Trans-Impedance Amplifier (CMOS TIA). The last choice is a good compromise between voltage and noise current face to Bipolar or Junction Field Effect Transistor (JFET) alternatives,

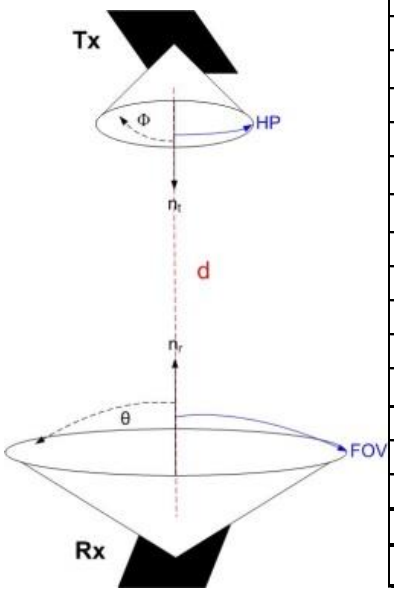
Emission is carried out with two wavelengths in differential mode, i.e. one wavelength is modulated by the signal according to one polarity and the other one is modulated with the inverted polarity. At the receiver, the two signals processed by the two photodiodes are therefore of opposite polarities and the subtraction of the second signal by the first one gives the possibility to obtain a global signal with a double amplitude (+6 dB).

The different noise contributions, that affect the two links and which result mainly from the transmission loss, are statistically independent; the noise level increases by 3 dB. The SNR therefore leads to a gain around +3 dB. In our configuration, for each wavelength, the signal is modulated and does not need complementary signal to achieve transmission. Differential modulation mode advantage lies by the capacity to suppress or strongly resorb broadband light jammers that could affect transmission.

Link Budget:

The prototype is an indoor full-duplex optical wireless communication link with Ethernet interface. The TX (LED)/RX (PIN PD) couple selection was motivated mainly for cost reasons, ease of implementation and especially integration capacity. Indeed, the goal is to maintain volumetric, energy and electrical constraints without having to change the fundamental electronic card characteristics and components on it. These choices have direct consequences on demonstrator functionality and especially on expected performances. For instance, from TX/RX features, it is possible to evaluate the optic link budget [17]. Figure 37 a) shows a Line Of Sight (LOS) link with the AP installed in the ceiling and the module at a given distance d and inside AP coverage area. This LOS configuration presents Interferences Inter-Symbols (ISI) limitation.

Figure 37 b) gives us the optical system parameters. If we want to maintain a positive link budget and a full duplex communication, the maximum distance is 0.25 meter. To increase throughput and distance, a TX (Laser)/RX (PD APD - Avalanche Photodiode) couple has a much more relevant potential. Special attention should be paid to the reception sensitivity module. It is a difficult exercise because it does not correspond in any case to the photodiode sensitivity value only. Indeed, it is necessary to take into account the beam concentration losses, optical concentrator and filters losses, and especially electronic module amplification, impedance adaptation, filtering, and digital/analog conversion. In our example, we go from -59 dBm to -25 dBm for reception sensitivity module and we assume 34 dB loss. We encountered difficulties to adapt the OWC module with the existing PLC plug electronic board.



Wavelength (nm)	850nm	950nm
Tx Power - Pt (mW)	60	55
Half Power angle - HP (°)	30	30
Tx angle/normal n^t - φ (°)	0	0
Rx Sensitivity - Se (dBm)	-25	-25
Field Of View - FOV (°)	15	15
Area Rx - A (mm^2)/normal n^r	4.00	4.00
Rx angle/normal n^r - Θ (°)	0	0
Distance - d (m)	0.26	0.25
m value (Lambert model)	4.82	4.82
n value (Lambert model)	20	20
Tx Power - Pe /φ (mW)	55.59	50.96
Area Rx Efficient - Aeff (mm^2)/ Θ	4.00	4.00
H0	5.48E-05	5.93E-05
Geometric Attenuation - Aff (dB)	-42.61	-42.27
Power Received - Pr (dBm)	-24.83	-24.87
Marging Link (dB)	**0.17**	**0.13**
Covearge area @ distance d (m^2)	**0.07**	**0.07**

Figure 37 - a) LOS optical link and b) Parameters (grey) and link simulation results

Setup and results:

Figure 38 shows PLC plug "tp-link" - AV 1300 Gigabit modified. The TX module is constituted by 850 and 950 nm LED. Each RX module is arranged with hemispherical lens, then passband optical filter and PIN photodiode. The global cost for each terminal or plug prototype is around 100 €. Due to power consumption needs (6 W), it is even possible to use terminal with a battery or plugged to USB port from laptop for instance

Figure 6. PLC plug "tp-link" - AV 1300 Gigabit modified

Figure 38 - PLC plug "tp-link" - AV 1300 Gigabit modified

Testbed result is shown on Figure 39. The test process is as following, from a maximum received power level, the signal is gradually attenuated by increasing the distance between the AP Plug and the Plug linked to user laptop via RJ45 port. We measured the optic level power only when there is no communication for 850 nm and 950 nm link respectively.

Throughput

The experiment highlighted several points. First, it is possible to benefit from HPAV2 standard characteristics (TDD, MIMO, OFDM, and CTC) in optical wireless communication device. It can be concluded that 850&950 association compared to the use of each wavelength separately can achieve higher throughput and higher distance. Additionally, data rate adaptation according to signal propagation modification offers robust link. The gains obtained are important, around + 50% in terms of throughput and + 30% for distance. A Front End Optic (FEO) modification by TX (Laser)/RX (Avalanche Photodiode - APD) couple will offer a better performance both in terms of data rate and in terms of distance.

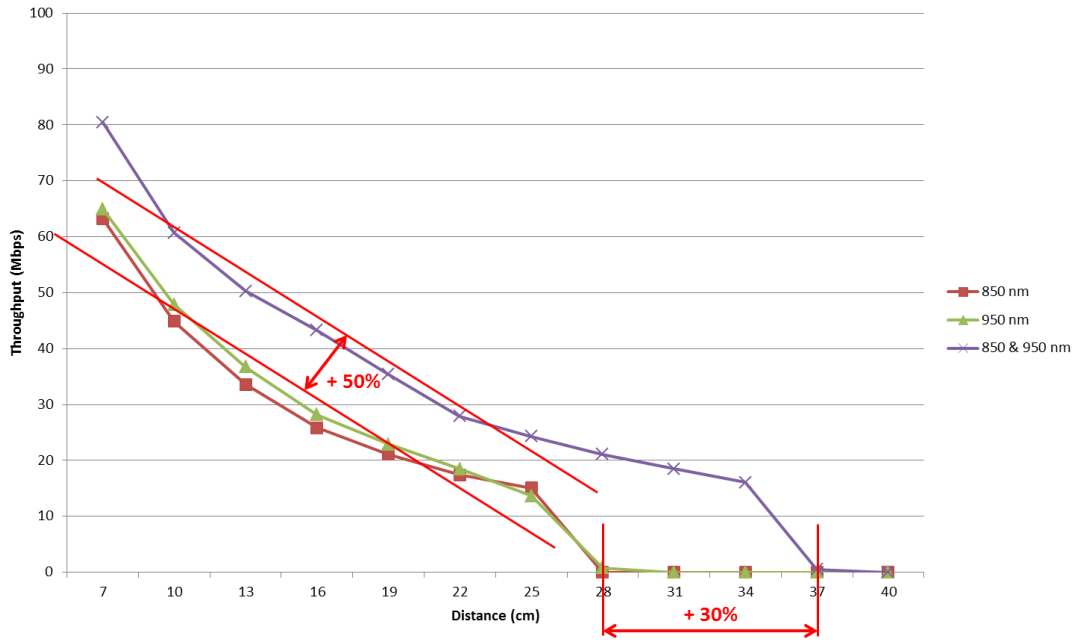


Figure 39 - Throughput versus Distance

Latency

As for latency determination, the classical Ping command on DOS mode is used. The result has shown an answer under 1 millisecond for a round trip, on both directions.

The experiment highlighted several points. First, it is possible to benefit from HPAV2 standard characteristics (TDD, MIMO, OFDM, and CTC) in optical wireless communication device. Then 850&950 association can achieve higher throughput and higher distance. However, the 1.3 Gbps data rate PLC protocol offer is no more than 250 Mbps on user layer, so we looking after alternative solution.

3.2.2.2 Optical Front-End

Two kinds of optical front-end are considered according to the demonstrator version.

Demonstration 1:

Visible Light Communications (VLC) has entered into the market in 2017 and Oledcomm and pureLiFi are offering solutions. Even if technological problems concerning industrialization have been solved, there still some others to solve. In the market solutions permit to offer symmetrical solutions of up to 43 Mbps. When compared with laboratory results [18] [19] [20], it can be rapidly seen as considerable difference in transmission rates. In this project a proof of concept (PoC) working in hard realistic conditions is to be used as a demonstrator. Two modulation techniques have been amply investigated for Multi-Gbps transmissions, the most common is Orthogonal Frequency Division Multiplexing (OFDM) [18] [19] [21], while a second one less common in Carrier-less Amplitude and Phase (CAP) [22]. Due to new standards in preparation, OFDM seems to be not only a commercial solution to PHY layer but also for this project. As OFDM is capable to manage multi-Gbps transmission rates, the questions that arise are: a) how to obtain a light source capable to deliver an energy budget that guarantee the link between Tx and Rx? We notice that ordinary white LEDs have a reduced bandwidth that doesn't permit to achieve high transmission rates. The second question is: how to ensure that the Optical Front End will get and amplify the low signal impinging the photodetector?
Some emitting sources [23] have been studied, microLEDs [24], blue lasers [25] and VCSL [19]. It has been decided to use an infrared (IR) laser [16] as required power obtained from modelling the scenario suggests powers up to 100 mW. Optical Detector Head (ODH), i.e. the light collector and the photodiode. It has been assessed the convenience of the Avalanche photodiode (APD) also used in EC project OMEGA [4]. Radiometric losses due to solid angle distribution in emitted energy and small size sensing area of the APD urge for the use of an adapted optical antenna. Table 13 shows three possible scenarios when three different half angles are used. From modelling, distance of 2 m and 1.5 m are taken into consideration. We also know that the emitting laser

source has a Lambertian behaviour. According to the parameters in Table 13 losses in the range of -25 to 42 dBm are foreseen (penultimate column) for angles ranging from 0 (direct signal) to 45 degrees. A different calculation suggests an increase in these loses by additional 5 dBm. It is possible to overcome the loss signal, by increasing the laser power just below the eye safety limit.

Case	Specifications						Laser Calculations				Optical detector calculations								
	HP (half power angle)	Distance (mt)	ϕ	Ψ	Pt (mW)	Se (dBm)	Lambertian order **m** (laser)	Radiant intensity **R(ϕ)**	Power of emision **Pe(ϕ)**	Half FOV (degrees)	Lambertian order **n** (detector)	**Area** (mm^2)	**Aeff(ψ)** (mm^2)	Gain **H0**	Collected power **Pr(ψ)**	Power of reception **Pr** (dBm)	**Marge**	**Aff**	**Link**
1	15	2	0	0	50	-35	19,99	3,34	167,06	7,5	80,67	78,53	78,53	6,56E-05	5,44E-03	-24,84	10,16	-41,83	Ok
2	15	1,5	0	0	50	-35	19,99	3,34	167,06	7,5	80,67	78,53	78,53	1,17E-04	9,67E-03	-22,34	12,66	-39,33	Ok
3	15	1,5	15	15	50	-35	19,99	1,67	83,53	7,5	80,67	78,53	4,79059	3,21E-06	1,28E-04	-37,95	-2,95	-54,94	X
4	22,5	2	0	0	50	-35	8,75	1,55	77,63	11,25	35,73	78,53	78,53	3,05E-05	5,28E-04	-28,17	6,83	-45,16	Ok
5	22,5	1,5	0	0	50	-35	8,75	1,55	77,63	11,25	35,73	78,53	78,53	5,42E-05	9,39E-04	-25,67	9,33	-42,66	Ok
6	22,5	1,5	23	23	50	-35	8,75	0,78	38,81	11,25	35,73	78,53	4,64095	1,26E-06	1,01E-05	-42,00	-7,00	-58,99	X
7	30	2	0	0	50	-35	4,82	0,93	46,30	15	19,99	78,53	78,53	1,82E-05	1,07E-04	-30,41	4,59	-47,40	Ok
8	30	1,5	0	0	50	-35	4,82	0,93	46,30	15	19,99	78,53	78,53	3,23E-05	1,91E-04	-27,92	7,08	-44,90	Ok
9	30	1	30	30	50	-35	4,82	0,46	23,15	15	19,99	78,53	4,42629	1,33E-06	3,41E-06	-41,77	-6,77	-58,76	X

Table 13 - Link budget calculations

Current work for demo-1 transmitter and receiver:

Given the 1 Gbps data-rate target of optical demonstrator-1, we suggested to use 200 MHz bandwidth source(s). First, we propose to use 200 MHz IR sources and complete transmitters from the past EC project OMEGA. Figure 40 shows a completed OMEGA-II transmitter and its optical front-end layout. The idea was to use these sources in the WORTECS optical demo-1 at an early stage of the project.

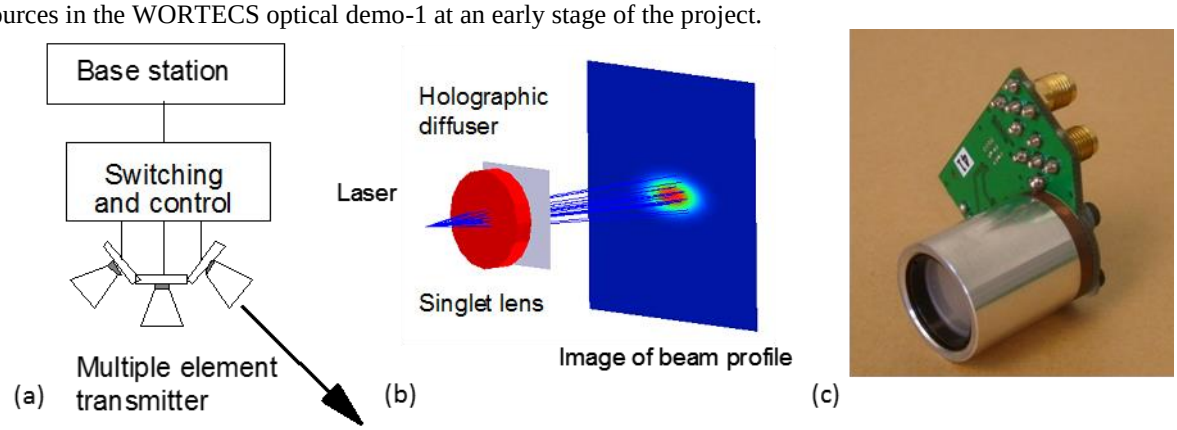


Figure 40 - OMEGA-II transmitter and source. (a) Multi-element transmitter, (b) Optical front-end layout and (c) Completed transmitter element.

The current driver IC is not suitable for high-speed linear driving as is required for OFDM, and investigation of different driving circuitry is currently underway.

Information on the preliminary transmitter design for demo-1:

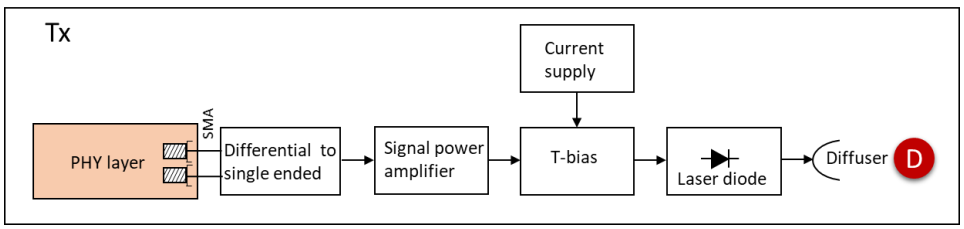


Figure 41 - WORTECS basic transmitter and source. Laser diode is the same as in Omega project.

Figure 37 depicts the basic configuration of WORTECS transmitter that integrates Omega's laser source. Tests carried out recently by Oxford team show that laser diode's cut-off frequency is greater than 400 MHz. Constant current laser source is under modification at Oxford, nevertheless a current source that can be used as replacement is specified in table 15b. In said table other main laser modulation frequency permits to get the througput goal established at 1 Gbps. Allow the modulating signal to pass through the laser. The said signal arrives in a digital format to a digital-to-analog converter (DAC). This last will deliver analog signal to a differential-to-single ended stage. A compensator (optional) would permit to linealize signal just in case a

decrease of transmission rate. Prior to T-bias we find the signal power amplifier. An alternative to Oxford's lased diode current supply is shown in table 14. All components works in the modulation band of IR laser diode (400 MHz). A rate of transmission of 4 bits/1 Hertz has been decided (Schematic of analog transmitter is in Fig 60, Appendix A2).

Component	MAX4444/5 Differential line receiver	AFT05MS003N RF power LDMOS transistor	THS4304 Wideband operational amplifier	Either Oxford or LD1255R	TAT7457 DE – 1200 MHz, 75Ω adj gain RF amplifier	LD1255R 250 mA Precision constant current laser driver	RLT860M-250MG High power IR laser diode
Stage (Refer to Fig. 37)	Differential to Single-ended conversion	Signal power amplification		Laser diode constante current driver			860 nm Transmission light source

Table 14 - Optical Tx components .

Information on the preliminary receiver design for demo-1:

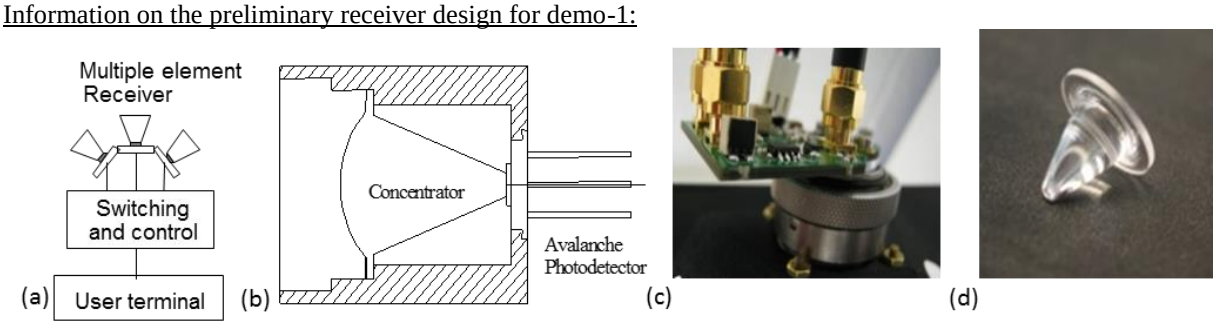


Figure 42 - OMEGA-II receiver. (a) Multi-element layout, (b) optical front-end layout, (c) completed transmitter element and (d) custom designed CPC.

Given the use of OMEGA-II transmitter in demo-1's preliminary design, the OMEGA-II receiver can also be used for the demo-1 receive side. Figure 42 shows details of the OMEGA-II receiver, where the optical front-end comprises an infrared filter, compound parabolic concentrator (CPC) and an APD (FirstSensor AD1900). The receiver has 30° FoV and a sensitivity of -38 dBm. Its bandwidth has been found to be greater than 200 MHz during the OMEGA project. The OMEGA-II receiver uses a trans-impedance amplifier (TIA) MAX3665 to amplify the output of the APD. Additional components such as priority encoder and demux are used on the receiver board to demodulate an OOK signal. In order to enable reception of the desired OFDM signal, digitisation of the output of the TIA must be performed and the additional circuitry for the OOK signalling can be removed/disconnected. The reception of OFDM signal has already been verified in laboratory.
From the Rx side and to overcome the loss signal a second solution consists in redesigning the optical collector (Figure 42b) to increase the light collecting area. The Compound Parabolic Concentrator (CPC) could be changed by a new free-form point concentrator (FFPC) as the shown in Figure 43. The main characteristics are that light fans arriving at up to 60° full angle are directed to the APD in a mean 85% once Fresnel and dissipations losses are taken into account. The F/# (or F-number means the ratio focal length over entrance pupil) can vary between 2.0 and 2.8 to guarantee total internal reflections (TIR) thus avoiding metallic thin films and extra production costs.

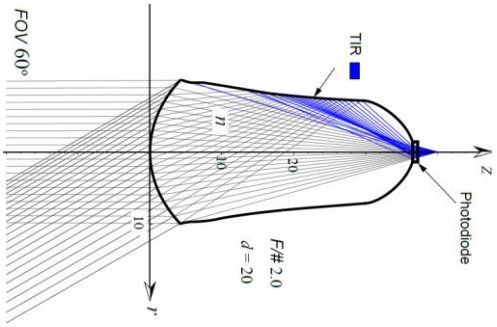


Figure 43 - WORTECS first version of receiver. F/# 2.0 and diameter equal 20 mm free-form concentrator.

This FFPC will have a collection area up to eight times bigger that the CPC and will ensure more signal into the APD. FFPC conducts the incoming signal into the APD shown in Figure 44 as photodiode. An analogic (electronic) circuitry block that consists in filtering, pre-amplification and conditioning of the signal permits to deliver the signal to the baseband stage (see §3.2.2.3).

AFE Receiver (Rx)

In Figure 44 the first element is a DC-to-DC converter that will polarize the APD. After the APD, a filter rejects noise and send an adapted signal to pre-amplification. A second filtering stage will further cleaning the signal. A variable gain amplifier (VGA) permits to adjust output signal level. This can be controlled directly by the PHY layer stage (Schematic of analog receiver is in Fig 61, Appendix A2).

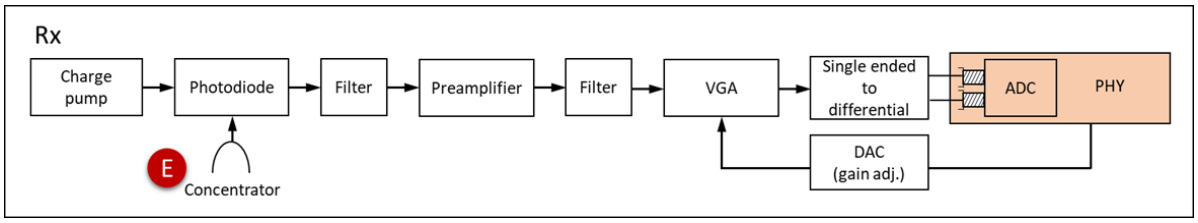


Figure 44 - WORTECS Rx Optical Front End.

Table 15 summarizes main components for Analog-Front-End. After arriving FFPC light is focused into an Avalanche Phtodiode (APD). Two APD are retained. First option is AD1900-8 TO from First Sensor already used in Omega project. Even if this APD is frequently out-of-stock, a supplier has been localized in France (Mouser). Its price, higher bandwidth and assessment makes him the first option. A second APD has been spotted at Hamamatsu (part S11519-30). Its advantage is the higher sensing area but price triples the first option. A second disadvantage is its higher breakdown voltage. APD needs a regulated gigh voltage DC to DC converter (charge pump) for APD ranging First Sensor and Hamamatsu APDs breakdown voltages. The selected device is shown in table 15.

Component	AD1900-8 TO or S11519-30 Avalanche Photodiode	CA05 Low noise, high voltage power supply	THS4304 Wideband Operational Amplifier	AD8367 Linear-in-dB VGA + MAX5141/4 DAC	THS4541 Differential Amplifier
Stage (refer to Fig. 40)	Light-to-current conversion	Regulated gigh voltage DC to DC converter (charge pump) for APD.	Filtering and Preamplification	Variable Gain Amplification + DAC for gain adjustment	Single-ended to differential amplification

Table 15 - Optical Rx components .

Filtering stages are included for instance, to filter out DC and swithching frequencies from DC-to-DC convertors; a preamplifier is conditioning the filtered signal and a second filtering stage filters out RF frequencies. The Variable Gain Amplifier permits to prevent the signal from saturation. From PHY layer, a digital signal is sent to VGA for this last to adjust the gain. An additional DAC is used to convert this digital signal in an analog input for VGA. The final stage consists in a single-ended to differential to prevent GND be used as reference.

3.2.2.3 Digital Front-End and baseband processing

OFDM has been used in many high data-rate applications, due to its architectural simplicity, robustness against fading in the propagation channel, and its spectral efficiency. Because of these advantages, OFDM modulation has been chosen in various standards.

For the optical link demonstration of WORTECS, OFDM is chosen as the modulation at 200 MHz bandwidth. The architecture of the transceiver follows standard OFDM system design with specification and parameters illustrated in Figure 45 described as following:

Tx Architecture

The Tx block diagram is shown in Figure 45 (top block). Specific parameters can be listed as:

- Scrambling based on IEEE802.11 standard

- Convolutional Coding at rates 1/2 and 3/4
- Bit interleaving based on the IEEE802.11 standard
- Symbol mapping as BPSK, QPSK, 16QAM, and 64QAM, based on the available SNR.
- Framing block deals with the pilot insertion (to be used for channel estimation and synchronization) and RF impairment estimation and compensation.
- The IFFT size can be any values between 64 to 256 points, and cyclic prefix (CP) can be set to 1/4, 1/8 or 1/16 or the IFFT size based on the channel condition.
- DAC is 12 bits resolution at 1 Gbps rate

Rx Architecture

The block diagram of the Rx architecture is illustrated in Figure 45 (bottom), which is basically the inverse of the Tx architecture, while the channel needs to be estimated as well to be used in detection process. The only block to be specified is the ADC as following:

- ADC with 11 bits resolution at 1 Gbps rate.

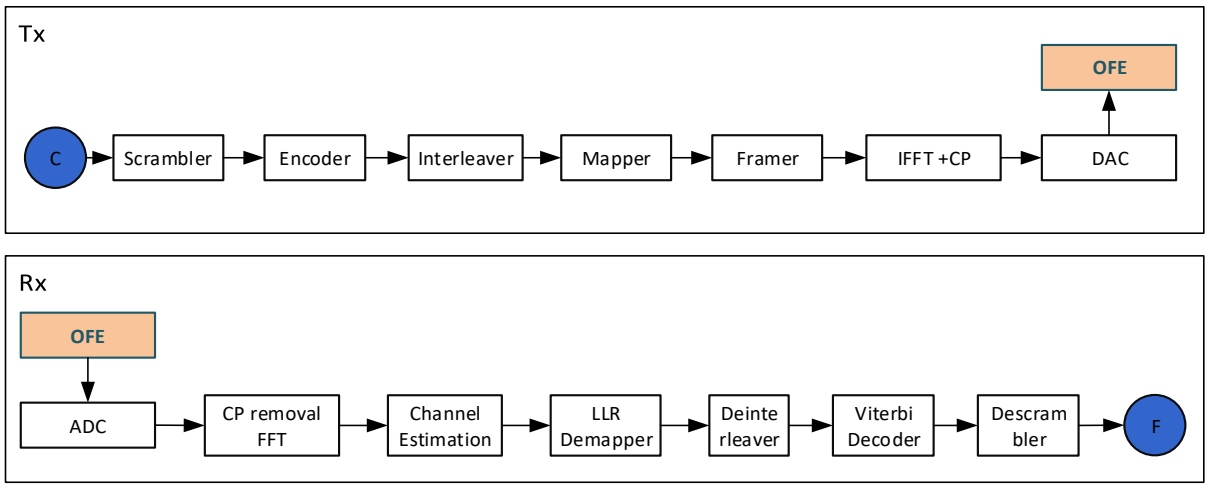


Figure 45 - Block diagram of baseband Tx and Rx architectures.

Lower MAC scheme

The lower MAC works as the interface between PHY and upper layers. For the demonstrator a proprietary access algorithm will be used with following specifications:

- Full-duplex operation
- Multiuser support
- Retransmissions and rate adaptation handling

Hardware specifications

The implementation board used for this proof of concept is Xilinx Zynq UltraScale+ MPSoC ZCU104 FPGA board, which features a Zynq® UltraScale+™ MPSoC EV device with video codec and supports many common peripherals and interfaces for embedded vision use case. The included ZU7EV device is equipped with a quad-core ARM® Cortex™-A53 applications processor, dual-core Cortex-R5 real-time processor, Mali™-400 MP2 graphics processing unit, 4KP60 capable H.264/H.265 video codec, and 16nm FinFET+ programmable logic.
The board is shown in Figure 46. Features and specifications of the board are as follows:
Configuration:

- USB-JTAG FT4232H
- Dual Quad-SPI flash memory
- MicroSD Card

Memory:

- PS DDR4 64-bit Component
- Quad-SPI flash
- Micro SD card slot

Control & I/O:

- 4x directional pushbuttons
- DIP switches
- PMBUS, clocks, and I2C bus switching
- USB2/3

Expansion Connectors:

- FMC LPC (1x GTH)
- 3 PMOD connectors
- PL DDR4 SODIMM Connector – 64 bit

Communication & Networking:

- USB-UARTs with FT4232H JTAG/3xUART Bridge
- RJ-45 Ethernet connector
- SATA (M.2) for SSD access

Power:

- 12V wall adaptor or ATX

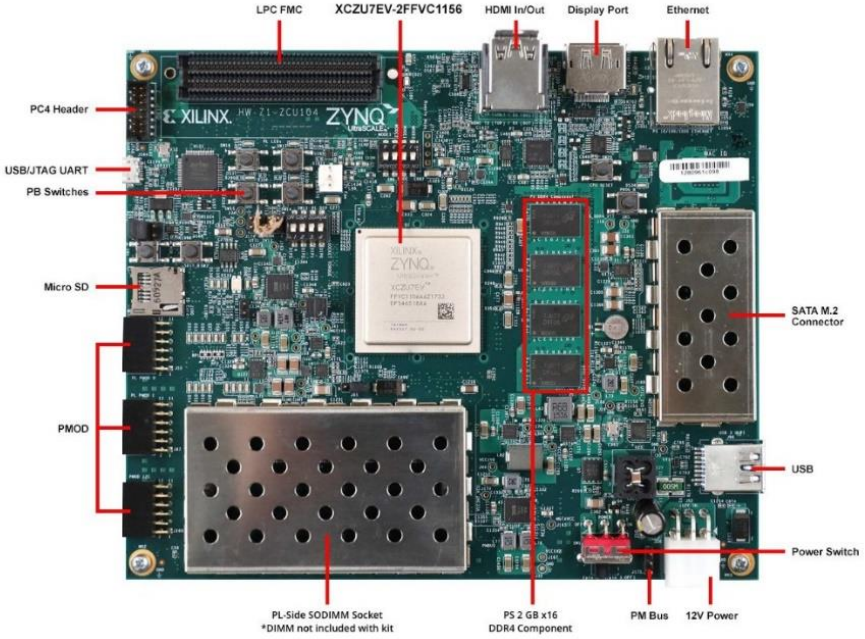


Figure 46 - FPGA board used for optical system baseband implementation.

3.2.2.4 MAC Medium Access Control considerations

The primary challenge addressed by WORTECS is the development of a system able to deliver ultra-high throughput (up to Tbps). In order to correctly specify these systems a survey of Medium Access Control (MAC) protocol state of the art has been undertaken and the synthesis is presented here-under.
The complete version is proposed on "WORTECS IR3.1_MAC Layer_v01.docx". This section will help towards MAC layer implementation final decisions that will be taken for Optical Wireless Communication Proof of Concept V1 and implementation purposes.
This complete version overview the following protocols: IrDA, OMEGA project MAC protocol, IEEE 802 protocol (802.11ad, 802.11ay, 802.11 SG Light Communication, 802.15.3, 802.15.7R1, 802.15.13 and 802.15 IG THz), IEEE 1901 – HomePlug, ITU (G.VLC and G.hn), Ethernet protocol (IEEE802.3), Flexible Ethernet and ETSI ISG NGP (Next Generation Protocol).
A key challenge for the WORTECS project is the development or an integration of an appropriate MAC layer, either by adaptation of existing work, or taking a new approach. The table here under presents a survey of solution that could be used following availability and maturity.

Proprietary LiFi MAC Architecture

The LiFi MAC used in this design is a modified version of the 802.11 PCF mode. The main distinction is that the LiFi MAC provides full-duplex operation. The full-duplex operation is enabled by the separate wavelengths used for the downlink and uplink. It is added that the LiFi MAC is not compatible with non-PCF stations. All the frame types and structures are the same as 802.11a, while the frame can support up to 16 stations connected to the access point.
The station to access point association process is rather different from the 802.11 MAC. The process is initiated by the access point with transmitting beacon frames periodically to check which stations are connected to the access point. Every station must respond within a given period with an ACK to the beacon frame. Upon receiving a beacon, the station attempts to connect to the access point via a 'connection request'. This connection request is not part of the 802.11 standard. The access point registers the station and starts polling it.
The LiFi MAC works by having a 'listen-then-talk' process, that is the station waits for permission from the access point to transmit information. If the station is not polled by the access point within a given period, then a

random back-off is used. On the other hand, if the access point does not receive a poll response for a specific period of time, the station gets removed.

Techno	Performances (Giga Bit per second)	Complexity	Maturity: • Pre-standard • Standard • IP • PoC • Chipset • Commercial	Cost	Availability	Result
IrDA	1 Gbps Giga-IR	5 Leds	PoC	Not available	Not know	*
OMEGA project MAC protocol	230 Mbps	Laser Class 1 & APD	PoC	Not available	No (only source code)	*
802.11ad						
802.11ay						
802.11 SG Light Communication	Several Gbps		Pre-standard		No	**
802.15.3	Several Gbps		Pre-standard		No	**
802.15.7R1	96 Mbps		Standard finalize 2018		No	*
802.15.13	Several Gbps		Pre-standard		No	**
802.15 IG THz	up to 1 Tbps		Pre-standard		No	**
G.VLC	Several Gbps		Pre-standard		No	**
G.hn	1,2 Gbps		Commercial	2 plugs Kit PLC 1 Gbps : 100€	Not know	*
Giga Ethernet	1 Gbps	PtP copper or Fiber	Commercial	Switch 24 ports+2 SFP: 150€	Yes	***
10 Giga Ethernet	10 Gbps	PtP copper or Fiber	Commercial	Switch 24 ports+2 SFP: 1500€	Yes	***
100 Giga Ethernet (25Gbps*4 λ)	100 Gbps	PtP Fiber	Commercial		Yes	***
Flexible Ethernet	200/400Gbps	PtP Fiber	Pre-standard 2.0		No	*
ETSI ISG NGP (Next Generation Protocol)	Several Gbps		Pre-standard		No	**
IEEE 1901 - HomePlug	1 Gbps		Commercial	4 plugs Kit PLC 1 Gbps : 100€	Yes	**

Table 16 - State-of-the-art MAC protocol to OWC overview.

3.2.2.5 Performance estimation

Simulation results (BER vs SNR)

The BER performance was simulated using BER curves for an optical OFDM with 64-QAM [26] and the already presented SNR map estimation. The resulting curves can be observed in Figure 47.

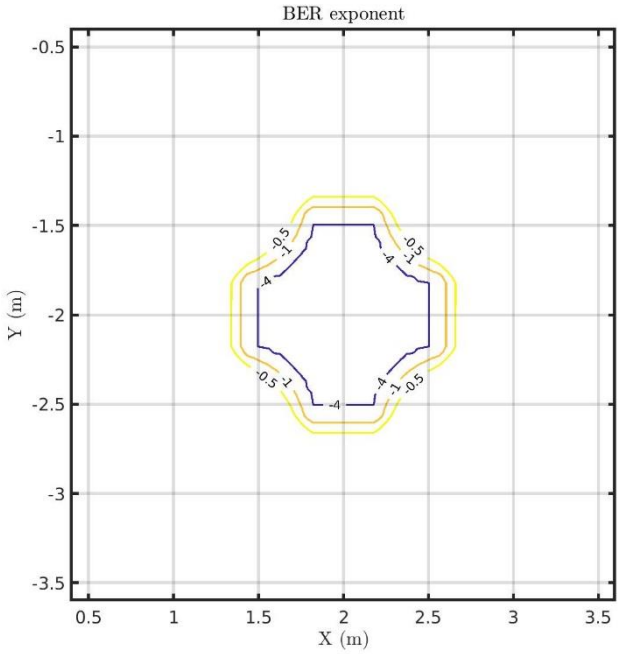


Figure 47 - Simulated BER for a 64-QAM DCO-OFDM using the parameters of Table 6.

Link budget

The OWC receiver will be optically designed to cover a FoV of 30°, in this manner and according to table 13 a reception power between -28 and -38 dBm is expected for distances ranging to metres in the best scenario to a distance of 1,5 m with Rx and Tx tilted 30° in the worst scenario.

Overall latency

The overall latency of the link is consisted of the latencies of each block along the Tx and Rx chains. For the digital baseband, the main latency is at the Rx processing. Depending of the error correction, channel estimation and equalization schemes, the actual latency of the system may alter. To have a sense of the latencies at the digital baseband PHY, assume the receiver processing cause 20 frames of latencies. This is not a far estimate, as long as a OFDM signal with large FFT size, e.g. 2048, and LDPC FEC is used. The OFDM frame length, depends on the FFT size, cyclic prefix and sampling rage. For an FFT size of 2048, with 25% cyclic prefix at 500 MSps, the frame period, TF will be

$$T_{\mathrm{F}} = \frac{500\times10^{6}}{2048}\times\left(1+0.25\right) = 5.12\ \mu\mathrm{s} \tag{9}$$

Therefore the overall latency of the digital baseband for this case can be estimated to be 20x5.12μs≅100μs. The remaining parts of the PHY, e.g. OFE, will have minor additional latencies, therefore it is safe to assume that the overall PHY (including lower MAC) incurs a latency of around 150μs.

The main contributors to the system latency however are higher layer protocols, such as interface drivers, etc. For instance, USB drivers can incur up to more than 1 ms latencies, and therefore if the transceivers use USB interface at one end, the RTT estimate can go up to 2 ms.

3.2.3 HW specification (Boards description, interfaces)

This section describes V1 demonstrator Tx and Rx architecture. In Figure 48the architecture of the OWC transceiver is shown. The transmitter Tx consist in an OFDM communication system with scrambler, encoder, interleaver, mapper and framer. The inverse fast Fourier transform (IFFT) stage contains a cyclic prefix CP, then the digital signal is converted to analog to feed AFE stages through a differential single ended. Though the T-bias the operational current and DC mounted signal is supplied to the laser diode. As for the receiver Rx, the concentrator optically amplify the incoming modulated laser light on the Avalanche Photodiode, which is in turn polarized by a charge pump. The signal has two filter stages and a variable gain amplifier. Through the single ended to differential stage the signal is delivered to the ADC. Note that the PHY DAC control the gain of the VGA. Symmetrically to the Tx, the FFT stage contains the code prefix removal. Channel estimation, deinterleaver and decoder are successively preparing the digital signal to be descrambled. AFE and PHY boards are separate and connected by SMA.

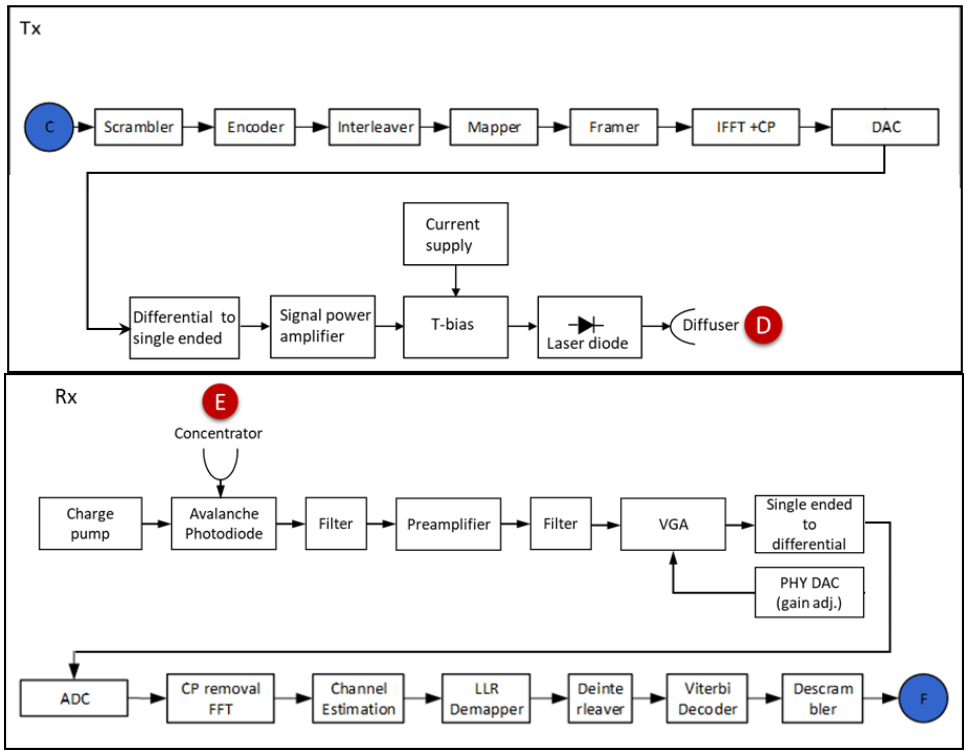


Figure 48 - Optical Tx and Rx schemes including Analog Front End and PHY layer

3.2.4 Fibre Wireless Fibre PoC v1

In order to provide sufficient network coverage, the narrow-beam FWF links rely on beam steering, localisation and tracking of the user terminals. Figure 49 shows a FWF setup in a generic form, where a beam steering unit (BSU) and location tracking unit is located at both the access point and the user terminal.

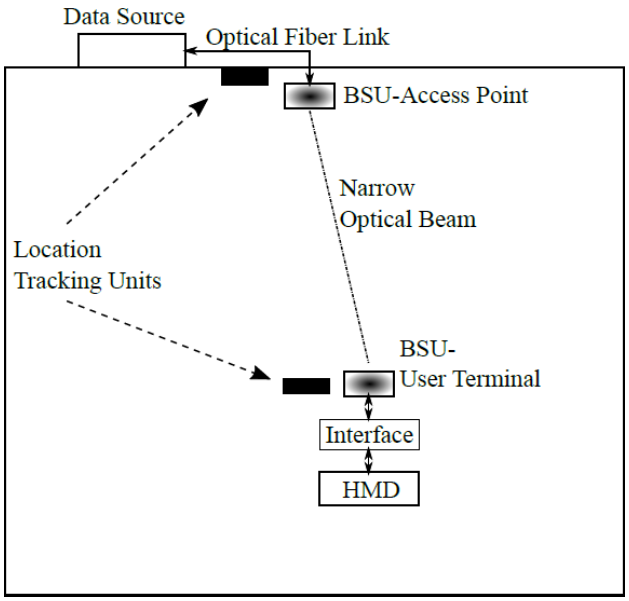


Figure 49: A Generic FWF link setup in an indoor environment (room cross section).

State-of-the-art fibre-wireless optical-fibre (FWF) concepts:

Ref.	Data Rate (Gbps)	FOV (°)	Coverage Area (m^2)	Tx-Rx Separation (m)	Steering Technique	Sample Rate, Modulation Format (N-WDM x Bits/sample x FEC overhead x Baud rate)
[23]	418	40 (±20)	3.745	3	SLM+AM	WDM, 14x4x0.93x8GB/s, 16-QAM
[23]	209	60 (±30)	9.424	3	SLM+AM	WDM, 7x4x0.93x8GB/s, 16-QAM
[24]	224	36 (±18)	2.985	3	SLM+AM	WDM, 6x4x0.93x10GB/s, 16-QAM
[24]	112	60 (±30)	9.424	3	SLM+AM	WDM, 3x4x0.93x10GB/s, 16-QAM
[25]	50	60 (±30)	9.424	3	SLM+AM	1x2x0.93x28GB/s, QPSK
[26]	50	45 (±22.5)	3.183	2.43	Lens, wide beam	4x1x1x12.5GB/s, OOK
[27]	36.7	29(±14.564)	1.325	2.5	Passive Diffraction Grating	1x1.6x0.93x23GB/s, DMT
[16]	10	34(±17.16)		2.5	1D Passive Diffractive Grating	10 Gbit/s, NRZ-OOK
[28]	1370	3mm (dia)		>1	No steering	4(OAM)x4(bits)x2(Pol)x**42.8GB**/s,16-QAM
[29]	10080			~1	No steering	12(OAM)x42(WDM)x2(pol)x**100Gbit**/s, QPSK
[30]	1280			~220	No steering	32(WDM)x40Gbit/s, NRZ-OOK

Table 17 - State-of-the-art FWF concepts.

Table 17 summarises the state-of-the-art FWF concepts, including the achieved data-rates, coverage area, transmitter-receiver (Tx-Rx) separation, steering technique and some details of the PHY. Many links have no coverage area, as they are fixed point to point examples. Ultrafast indoor OWC demonstrations have been reported over Fibre-Wireless-Fibre (FWF) link geometries [27], [28]. FWF laboratory experiments have achieved Tbps data rates using orbital angular momentum (OAM) multiplexing techniques and coherent transmission. [29], [30]. Single-mode fibre (SMF) transceivers have typically been used, although multi-mode fibre (MMF) realizations have also been successful [31].
Some research efforts have focused on enhancing the coverage area. Wang et al. [20] achieved a 4 x 12.5 Gbps link with a relatively large coverage are of >3m^2, however, the demonstration was not bi-directional and the receiver needed to be normally oriented to the incoming beam direction. Koonen et al. [32] also designed a FWF link with a high data rate of ~37 Gbps. However, the coverage area was small and, again, the receiver had to be aligned normally to the incoming beam.
Recently, UOXF in collaboration with University College London achieved both ultrahigh data rates (400 Gbps) and wide coverage [33], [34]. These demonstrations incorporated beamsteering units at both ends of the link with adaptive optics compensation [35]. These are the fastest wireless links (RF or optical) demonstrated thus far, with practical indoor coverage.

Current plan for FWF links in WORTECS:
The aim of the optical demonstration-2 is to provide point-to-multipoint FWF communication links achieving 1 Tbit/s with automated alignment capability for the smart cave shown in Figure 5. Key tasks around the demonstration-2 are as following:

Task 1: Localisation and Tracking
Currently, a review of the state-of-the-art localisation and tracking techniques is underway along with an investigation into the use of a portable camera, Pixycam, as this could provide a cost effective solution. Pixycam's performance evaluation is in process focusing on coverage, accuracy and wavelength of operation. Depending on the findings of this evaluation, the next step could be investigation into tracking and beam-steering. The HMD uses a localisation system, called the LightHouse [36], purely for application purpose to know the location and orientation of the HMD. An investigation into the use of this existing localisation system for aligning the optical communication beam will also be carried out.

Task 2: FWF optics for Tbit/s links
In order to achieve wide FoV optical demonstration-2 will build on the previous work at UOXF [27] and investigate use of an OptoTune beam-steering mirror which, in addition to providing large FoV, could lead to an improved link budget in comparison to previously used angle magnification technique for beam-steering.
In order to provide 1 Tbit/s, the use of discrete multi-tone (DMT) modulation, polarisation diversity and wavelength division multiplexing (WDM) with more than 14 channels will be investigated. Investigation in to point-to-multipoint links will be carried out through the use of passive split and spatial light modulators (SLMs).
A long-term aim within this task will investigate into a compact FWF system, which can be easily integrated into VR HMD and the network to be designed in WORTECS project. Focus of this long-term aim will be on a FWF prototype which is transportable and data-rate requirements can be relaxed.

3.2.5 Potential risks

On OWC V1: Costs of prototyping can increase due to lack of main components availability. A first case has arisen with APD used in receiver. The envisaged APD was out-of-stock or out of production. In such a case special optical concentrators are designed and some samples produced. These kind of unexpected delays results is looking for new solutions. AFE has identified risks for APD and IR laser diode. In both cases solutions are ongoing.
OWC V2: The prototype requires a special and non-existing Optical Link device. University of Oxford works in this solution. Oledcomm and University of Las Palmas have studied the specifications and are expectants to contribute to solution if needed.

4 Sub- Layer 2.5

The IEEE 1905.1 standard introduces a new sublayer 2.5 to support heterogeneous technologies, such as Power Line Communication or Wireless LAN, in home networks. This new abstraction layer sits just above the data link layer (see Figure 50) and hides the diversity of MAC implementations. Further, the sublayer 2.5 can switch between these underlying MAC technologies to reduce latencies and increase throughput.
In WORTECS project we also investigate heterogeneous network links, radio and optical, and want benefit from features supported by layer 2.5. Therefore, we follow the idea introduced in the IEEE 1905.1 standard and implement it on our hardware platform.
The major difference between IEEE 1905.1 and our project are the user requirements. As depicted in Figure 50, the IEEE standard considers only home networks with technologies like IEEE 802.11 Wireless LAN, IEEE 1901 Power Line Communication, and IEEE 802.3 Ethernet. These technologies support network throughput up to 1 Gbps. In WORTECS project, however, we consider Virtual Reality scenarios with 1000x higher network throughput! These new requirements cannot be satisfied with solutions introduced in the IEEE 1905.1 standard and various innovative approaches must be examined.

Figure 50 - IEEE 1905.1 standard supports heterogenous home networks by adding a new sublayer that sits on tome the MAC layer (layer 2)

4.1 Implementation constraints

The sublayer 2.5 introduced in the IEEE 1905.1 standard support scenarios with a network traffic of 1 Gbps. A standard processor used in personal computers, for example Intel i7, is capable of processing frames fast enough to support such network speeds. Therefore, the layer 2.5 implemented as a software can support scenarios with a network throughput of 1 Gbps. For example, in our previous project OMEGA we implemented the InterMAC, the predecessor of IEEE 1905.1 sublayer 2.5, for the Linux kernel (that is, a software implementation) and achieved data rates up to 930 Mbps [32], The InterMAC implementation needed about 7.5 microseconds to process a single frame, so it was capable of forwarding frames with 1.5 Gbps, provided frames are at least 1400 bytes long.

In this project, we consider scenarios that require up to 1 Tbps throughput. Clearly, software implementations of Layer 2.5 cannot support such high throughput, since a single frame must be processed within a few nanoseconds. Further, even hardware implementations could hardly support this and in this project we intend to examine potential solutions and limits for such challenging task.

Current FPGA platforms work typically with a clock of hundreds MHz, so a single clock cycle is a few nanoseconds. Therefore, the FPGA implementation must process at least one frame in a single clock cycle. The only way to support such fast packet handling in parallel processing, depicted in Figure 51. In this project we investigate the benefits and limits of parallel processing in the sub-layer 2.5 implementation.

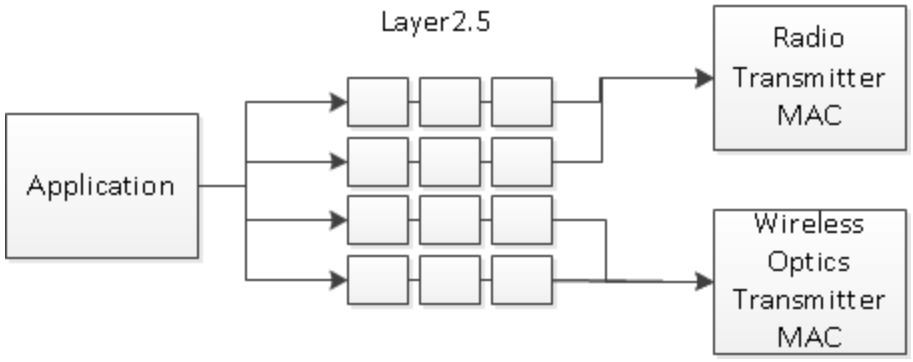


Figure 51 - Parallel hardware implementation to support frames processing within a few nanoseconds

Another solution to support high-speed networking is an appropriate architecture of packet processing. Time critical operations, mainly packet forwarding, is done in the DataPlane (DP), and all other tasks in ControlPlane (CP). In short, DP receives frames on a certain interface, looks up the forwarding table and sends them to a specific outgoing port. This forwarding table is updated by CP, which runs various algorithms to find a fast connection between network devices.

Since DP includes time-critical operations, it requires a very efficient implementation, based on FPGA platform in this project. The ControlPlane, however, does not have such challenging timing constraints and can be implemented as software to provide more flexibility.

We will base our DP implementation on the Xilinx FPGA board VC709 (see Figure 52). The ControlPlane will be a software solution, running on a Linux-based PC, connected to the DataPlane via an Ethernet port. This FPGA board supports four 10 Gbps Ethernet ports, with an option to add another four interfaces on an extra

expansion card. Although this board will not support 1 Tbps network forwarding, due to limits in physical interfaces, we will use it to investigate various hardware solutions for the sub-layer 2.5 and carry out performance tests of FPGA-based packet process this extra abstraction layer.

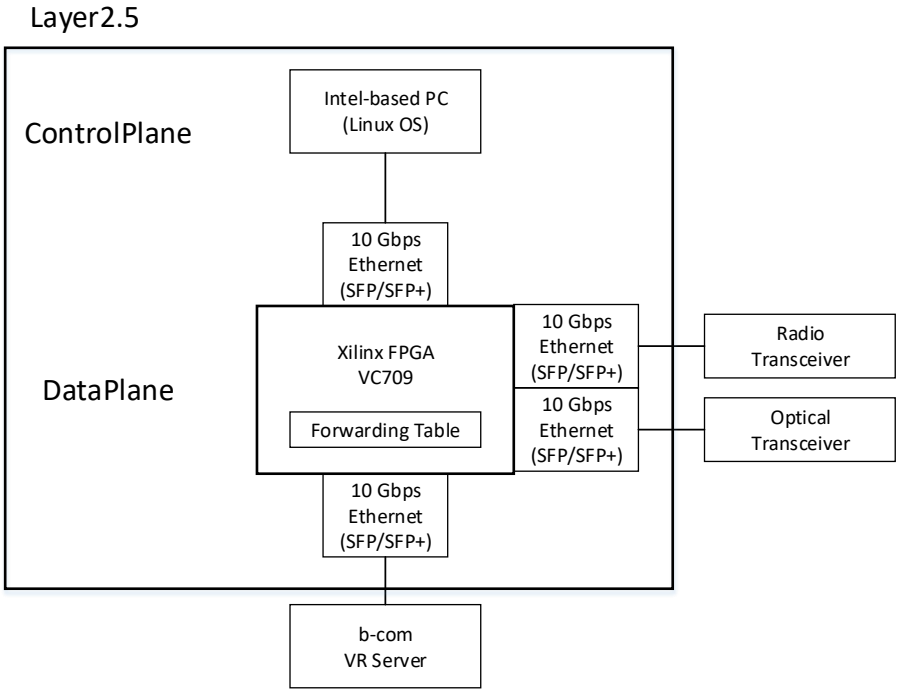


Figure 52 - Hardware architecture of Layer2.5

4.2 Latency constraints

To support low-latency communication in Virtual Reality scenarios, the Layer 2.5 must process frame fast enough. According to the Table 2 the most demanding VR scenario requires raw data rate of 120 Gbps with a low latency data compression. If the VR application uses a typical frame size of about 1.5 Kbytes, then each frame must be processed within 0.1 microseconds, that is, in about 20 FPGA clock cycles if the FPGA frequency is about 200 Mhz. As stated before, the sub-layer 2.5 based on parallel processing may be capable of supporting such high network speeds and it will be investigated in this project.

4.3 Potential Risks

Since our implementation of the DataPlane for FPGA platform is only a prototype, it will have several limitations. For example, incoming frames must be at last 72 bytes long and aligned to 64-bit boundaries. For frames not fulfilling this requirement the FPGA will add extra padding bytes. In general, these extra bytes do not cause problems with typical TCP/IP applications but there is still a risk that some application will not handle such frames properly.
Further, there is a risk that application will be using some extra protocols, like spanning tree or multicast, which must be carefully handled by each network device. As we do not plan to implement extra protocols on the DataPlane, such applications may not work.

5 Video processing

5.1 Video / MAC layer interconnection

As described in chapter 1.3, the generated video signal is not compatible at all with IP signals required at the MAC layer input.

A specific module should realize this adaptation and could be enriched with a video compression section to make it compatible the video data rate and the wireless bandwidth. For extended compatibility, a variable compression rate could allow to use wireless systems that have different bandwidth.

5.1.1 Existing components

5.1.1.1 Passive HDMI to RJ45 extender

The first thing to do is to look at what already exist. A first product can be found that convert HDMI port onto eth one.

Figure 53 - Passive HDMI to RJ45 Extender

This system is a simple connector adaptor in order to avoid using HDMI expensive cables. In place, a more common Cat5e/6 Ethernet cable can be used.
The supported bandwidth is only limited by the Ethernet cable capacity. Commonly, 1080p video signal could be injected.
But this system do not convert Video signal in any manner. That means the signal going out from the RJ45 port is not packet oriented as the MAC layer needs.

5.1.1.2 Active HDMI to Ethernet extender

Another component already exist. It is an active component that extract the video from the HDMI protocol, and reformat using packets and send them onto an 1Gb ethernet link.
This kind of component can be found for 50€:

Figure 54 - Active HDMI to RJ45 Extender

They support switch and router on the Ethernet link, but only accept 1080p 60fps because of the Ethernet 1Gb bandwidth limitation.
To allow higher resolution, like 4K 30fps, compression is introduced, to reduce the video data bandwidth to less than what the GbEth port can accept. The problem is the compression latency. These module are mainly used to allow a long distance between the source and the display, and if the signal takes 100ms to reach the destination, it is not noticeable. But in our case, the latency budget is close to 2ms, so this kind of common compression algorithm cannot be used.

5.1.2 Specific components

As no element already existing can realize the function we needs, a specific module should be design.

This module will be realised in an FPGA board because of the challenging data rate that must be manipulated and because of the short latency budget available.
Because of the b<>com developers skills and experiences, an Intel FPGA base board will be used.
The following schemes present the different processing to realise.

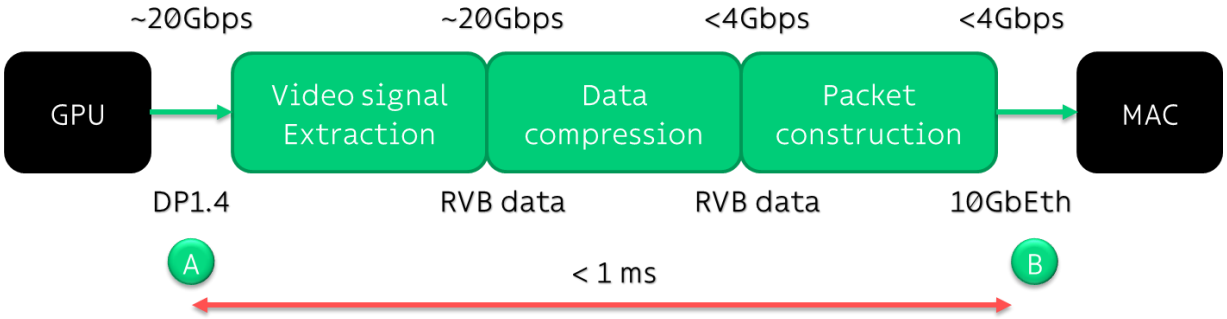


Figure 55 - GPU to MAC connection

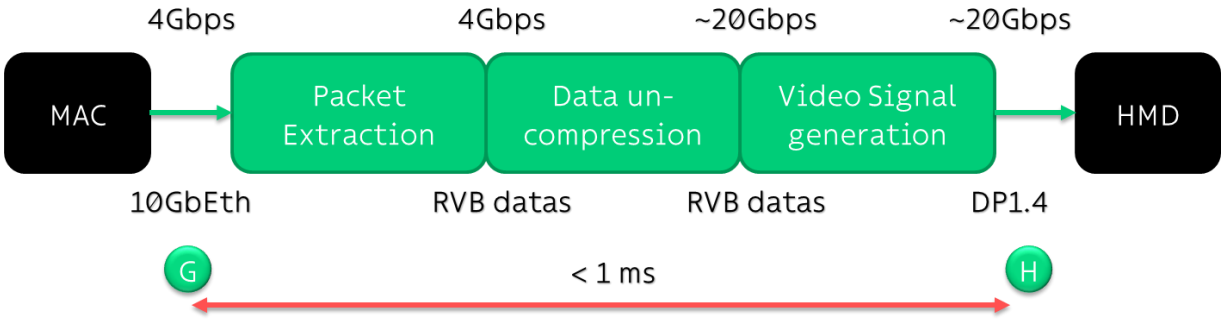


Figure 56 - MAC to HMD connection

5.1.3 Video extraction

First of all, video data from the graphic card should be extracted from the transport layer.
To realise that operation, a first solution could be to use the high speed FPGA serdes embedded in the nowadays high end FPGAs. These serdes have a high data rate of 12Gbps per link, higher than the DP data rate per lane.
Intel and Xilinx provide both software IP that are compatible with DP standards. The problem is that the video formats they support are mostly linked to standards like UHD 4K or even 8K. However, it is not clear at all that VR definition could be compatible with that IP. Furthermore, previous design with similar principle, clearly demonstrates that the clock recovery from the graphic card video signal is not trivial at all.

A second solution could be to realise a homemade daughter card with:

- DisplayPort IOs, one input and one output
- A standard compliant video receiver and transmitter
- FMC connector to link the video components to the FPGA

Such a solution allows a full compatibility with the complex DP standard, and by the way, the VR video resolutions. That solution avoid the risk of software IP compatibility and reduce the hardware trouble encountered with clock recovery in such high speed serdes. Research to identify the best components is ongoing, but the preliminary results show that there is only a few number of available reference on the market.

5.1.4 Video compression

Considering the total amount of data to transfer to the HMD on one side, and the maximum wireless link throughput on the other side, a compression phase will be mandatory to fit the wireless system bandwidth. Compression ratio will be selected accordingly to the radio and optical wireless link capacity.
The quality loss in the compression phase should be at small as possible, but if the compression ratio is too high (>8) a quality loss could be tolerated.
The most critical point on this process is the latency required to realise such a compression. In this project, with an overall latency of 17ms, only few milliseconds could be allowed to this phase.
By the way, all the classical algorithm base on H264 (MPEG4 AVC) or h265 (HEVC) could not be used because of the long time it takes to analyse and treat each pictures, even if executed on FPGA.

A good candidate has been identified in the intoPix provider. They developed a software IP based on TICO (tiny codec), and ready to use in an FPGA. The maximum resolution and frame rate are greater than the one required by the Pimax8K, the compression latency is smaller than 18 lines and the decompression latency smaller than 11 lines. That's means, for a resolution of 2x2560x1440@90Hz, a compression + decompression budget of approximatively 230µs (1/90/1440*(11+18)).

5.1.5 Packet creation

The last step of this module is feeding a 10Gb Ethernet section with the compressed data generated by the Intopix IP. This interface could be realised using a soft IP in the FPGA and its high-speed serdes. At this point, the creation of a destination IP address is required.

5.2 USB/MAC layer interconnection

Similarly to what has been done on the downlink (interconnection between video and IP interface), the same adaptation should be done on the uplink, between USB and IP interfaces.
In order to limit hardware resources, the same FPGA platform as in 5.1 should be used.

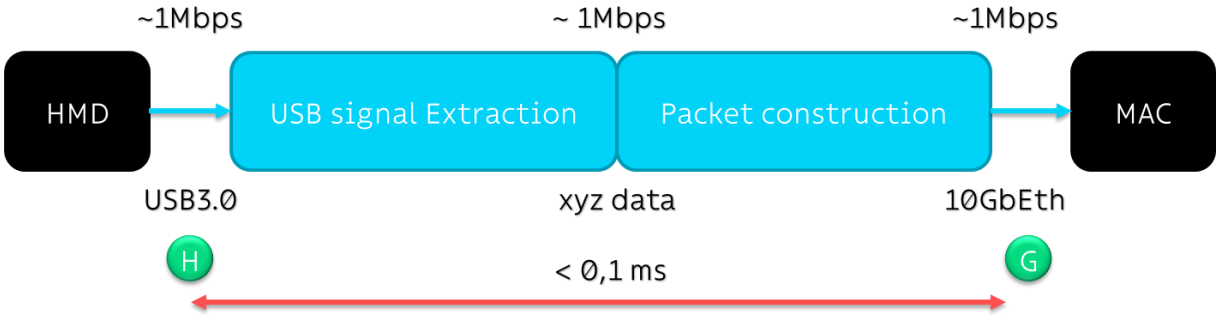


Figure 57 - HMD to MAC connection

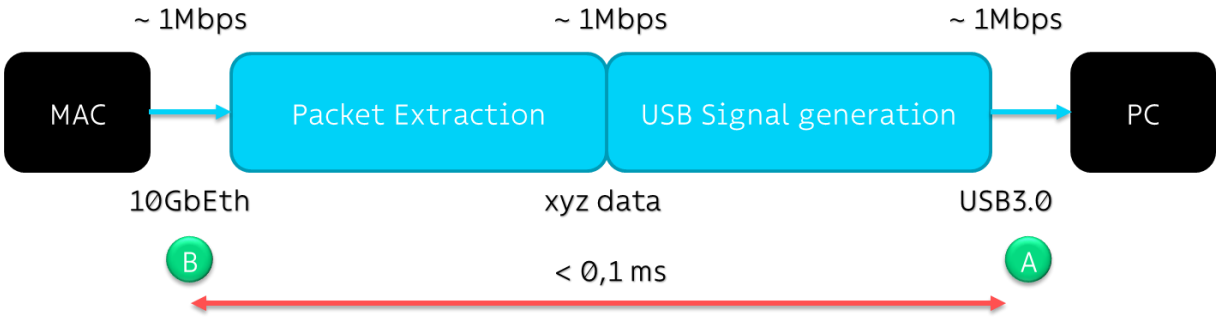


Figure 58 - MAC to PC connection

6 Heterogeneous Network

Orange is trying to find a solution with Cisco in order to manage a fast switching on layer 2 (Ethernet protocol).

6.1 Orange proposal

Layer 2 roaming (Ethernet) and low-latency management with 2 features is of great importance to be validated with CISCO.

1) Real time Mac-learning

a)Level 2 equipment (Ethernet Switch) must immediately detect VR headphones (HMD) roaming connected wirelessly from one AP to another.

b) Learning the mac address from port A to port B must be done in real time. As a reminder, mac learning requires to receive traffic from HMD port to achieve association source MAC/port for the switch.

2) Real time changes Mac notification

a) For geo-loc needs, VR server needs to know HMD exact position in the game environment.

b) It must be notified in real time HDM mobility events (mac address) on Ethernet switch.

c)A notification/telemetry mechanism from the switch to the VR server must stream as quickly as possible HMD movement information to a new port of the switch (streaming telemetry notion).

As a reminder, the operating constraint of this sequence is dictated by the VR application, and is extremely restrictive in terms of budget "time" < 3 msec .

The learning combination Mac/new Port + motion notification must fit into 3 ms maximum. At first glance, an "on-demand" telemetry mechanism (state change operational notification on a Table in the CAM) would be targeted. However, a number of points must be confirmed:

-Mac-learning responsiveness (TBC)

-Available telemetry mechanism and L2 mac table (TBC) data model

-Notification mechanism responsiveness (aka "Event Driven Telemetry")

-Applicant platform if previous needs can be made WITH the constraints mentioned above.

Up to now, there is no Cisco commercial equipment available and able to manage the upper requests.

There is still regular meeting with Cisco to see how to find a solution within WORTECS project lifetime.

6.2 IHP proposal

The major feature of Layer2.5 is to switch from one technology to another when it is needed and desired, to enable continuous data transmission to the user. For example, when the user moves inside a room it leaves the coverage of a certain optical or radio access point (AP) and should start receiving data from another AP. Further, in case of link degradation the Layer2.5-based switch selects another technology, with a better performance, for data transmission. These changes in technologies or access points are named handovers.

From the switch perspective, a handover is just an update of the internal switch table, which determines to which outgoing port frames are forwarded. The main challenge is to figure out when the handover (the update of the switch table) should happen and what is the next outgoing port for certain frame types. We consider the following two solutions for handover decisions

1. MAC address learning

On some technologies, for example the optical communication considered in this project, access points performs handover on their own. In this case, however, the downlink communication (towards the user) does not work after handover, since the switch keeps sending data to the “previous” access point. Therefore, just after the handover either the user or the corresponding access points should send a frame towards the switch. Then, the switch detects that user data arrives from a different port and updates the switch table.

2. Active link monitoring

To determine the link quality of several connections the Layer 2.5 sends probe frames. It allows estimating mainly link delay and packet error rate. With these link characteristics switch can initiate handover to find better links than the current one. However, this approach requires some feedback from the user network device, and therefore we would probably use common ICMP messages (e.g. ping) to estimate link quality.

In the next step we consider underlying technologies, optics and radio, and also end-user devices to define the most effective way to carry out handovers in virtual reality scenario of the WORTECS project.

6.3 pureLiFi proposal

pureLiFi proposal only concerns the handover from one LiFi AP to the neighbouring AP when the user moves from the coverage area of one to another. Thus, the major feature of Layer2.5 would be to fast switch from one AP to the other. The handover process in the LiFi cellular network is handled by the AP. Considering the handover duration, the APs involved in the handover can inform the switch regarding the dropped or the established link to the user. This can be done using the user and involved APs MAC addresses. The switch then can update its internal switch table to determine to which outgoing port frames are forwarded to, as described in the previous subsection.

6.4 Synthesis

Here below, the different proposals for heterogeneous network are presented. Note that pureLiFi solution is not a Heterogeneous Network solution because it works on LiFi handover.

	ORANGE	IHP	pureLiFi
Proposal	Cisco switch (Ethernet)	Owner	Owner
Data rate	Nx1 Gbps Or 10 Gbps (N=12, 24 or 48 ports)	5-10 Gbps per lane	
Latency	<3 ms (to confirm)	<1 ms	
Switch process	Based on no link (On/Off)	Based on no link detection and probably on link quality (PER, delay)	RSSI
Other features (Geolocation, size, cost, …)	-Geolocation linked to the port address -24 ports 10/100/1000 + 4 SFP -Size 1RU -Public price 2K€	DataPlane in FPGA Virtex7	

Table 18 – Heterogeneus network synthesis.

7 Conclusion and perspectives

This internal report describes the main challenges that the Wortecs project has to achieve and the main solutions which are being investigated to implement the VR optical and radio demonstrations. First, the report recalls the main requirements in term of throughput and latency for achieving VR transmission. The report highlights interest about location measures, since bad location estimation leads to bad VR transmission. Then, a description of the environment, where the demonstration will be carried out was provided. From this description, a channel model has been proposed to simulate the system and to evaluate some performance especially in terms of link budget. Then, the optical and radio architecture is presented by describing all the interfaces that have to be taken into account to interconnect all the equipment of the demonstration. A focus about the potential HMD to use is made showing that connector and video resolution are key elements that condition the transmission chain. Then, the report focuses on both optical and radio technologies that are foreboded to be implemented in respective demonstrators. Both analog front-end and digital parts are described. Some solutions are always in studies but decision will be done as soon as possible. The analysis of mutualized optical and radio architectures is also done, showing that common parts could be combined to diminish the development. However, an adaptation of the parameters has to be done and a flexible and fast reconfigurable HW to be design.
Then, description and some proposal about the MAC layer complete the global system overview. Following the optical and radio data throughput that can be achieved by the V1 demonstrator and the video format supported by the HMD, data compression and encapsulation are needed requiring some HW developments.

8 References

[1] J. Lopez-Hernandez, R. Perez-Jimenez and A. Santamaria, "Modified Monte Carlo scheme for high-efficiency simulation of the impulse response on diffuse IR wireless indoor channels," *in Electronics Letters,* vol. 34, no. 19, pp. 1819-1820, 1998.

[2] J. Rufo, J. Rabadan, V. Guerra and R. Perez-Jimenez, "BRDF Models for the Impulse Response Estimation in Indoor Optical Wireless Channels," *IEEE Photonics Technology Letters,* vol. 29, no. 17, pp. 1431-1434, 2017.

[3] A. Ramirez-Aguilera, J. Luna-Rivera, V. Guerra, J. Rabadan, R. Perez-Jimenez and F. Lopez-Hernandez, "Multi-wavelength modelling for VLC indoor channels using Montecarlo simulation," *10th International Symposium on Communication Systems, Networks and Digital Signal Processing (CSNDSP), Prague, 2016,* pp. 1-6, 2016.

[4] D. O'Brien and al, "High-Speed Optical Wireless Demonstrators: Conclusions and Future Directions," *Journal of Lightwave Technology,,* vol. 30, no. 13, pp. 2181-2187, 2012.

[5] J. C. Zhang and H. Zhang, "Near-infrared green camouflage of cotton fabrics using vat dyes," *Journal of the Textile Institute 99.1,* pp. 83-88, 2008.

[6] M. Janecek, "Reflectivity Spectra for Commonly Used Reflectors," *IEEE Transactions on Nuclear Science,* vol. 59, no. 3, pp. 490-497, 2012.

[7] J. Armstrong and B. Schmidt, "Comparison of Asymmetrically Clipped Optical OFDM and DC-Biased Optical OFDM in AWGN," *IEEE Communications Letters,* vol. 12, no. 5, pp. 343-345, 2008.

[8] A. Rabl, "Optical and thermal properties of compound parabolic concentrators," *Solar Energy,* vol. 18, pp. 497-511, 1976.

[9] R. Winston, L. Jiang and M. Ricketts, "Nonimaging optics: a tutorial," *Advances in Optics and Photonics,* vol. 10, no. 2, pp. 484-511, 2018.

[10] T. Mohsnein, D. Truong and B. Baas, "Low-Complexity Message-Passing Algorithm for Reduced Routing Congestion in LDPC Decoders," in *IEEE Transactions on Circuits and Systems,* 2010.

[11] A. Li, L. Xiang, T. Chen, R. Maunder, B. Al-Hashimi and L. Hanzo, "VLSI Implementation of Fully Parallel LTE Turbo Decoders," in *IEEE Access,* 2016.

[12] B. Tahir, S. Schwarz and M. Rupp, "BER comparison between Convolutional, Turbo, LDPC, and Polar codes," in *2017 24th International Conference on Telecommunications (ICT),* Limassol, 2017.

[13] A. Stimming, P. Giard and A. Burg, "Comparison of Polar Decoders with Existing Low-Density Parity-Check and Turbo Decoders," in *IEEE Wireless Communications and Networking Conference Workshops (WCNCW),* San Francisco, CA, 2017.

[14] P. T. G. Bouchet, "Acemind new indoor full duplex optical wireless communication prototype," in *SPIE Optics and Photonics,* San Diego, 2016.

[15] D. Y. Y. Y. Z. Song, "An indoor broadband broadcasting system based on PLC and VLC," *IEEE Transactions on Broadcasting,* June 2015.

[16] J. X. C. B. Khalighi, "Double laser differential signaling for suppressing background radiations in FSO systems," in *25th Biennial symposium on communications,* Ontario, 2010.

[17] Bouchet, Wireless optical Communication, Wiley, 2012.

[18] H. Chun, S. Rajbhandari, G. Faulkner, D. Tsonev, E. Xie, J. James, D. McKendry, E. Gu, M. D. Dawson, D. C. O'Brien and H. Haas, "LED Based Wavelength Division Multiplexed 10 Gb/s Visible Light Communications," *J. Lightwave Technol,* vol. 34, pp. 3047-3052 , 2016.

[19] H.-H. Lu, Y.-P. Lin, P. Wu, C. Chen, M. Chen and T. Jhang, "A multiple-input-multiple-output visible light communication system based on VCSELs and spatial light modulators," *Opt. Express ,* vol. 22, no. 3, pp. 3468-3474 , 2014.

[20] C. W. Oh, E. Tangdiongga and A. M. J. Koonen, "Steerable pencil beams for multi-Gbps indoor optical wireless communication," *Opt. Lett,* vol. 39, pp. 5427-5430 , 2014.

[21] A. H. Azhar, T. Tran and D. O'Brien, "A Gigabit/s Indoor Wireless Transmission Using MIMO-OFDM Visible-Light Communications," *IEEE Photonics Technology Letters,* vol. 25, no. 2, pp. 171-174 , 2013.

[22] Y. Wang, L. Tao, X. Huang, J. Shi and N. Chi, "8-Gb/s RGBY LED-Based WDM VLC System Employing High-Order CAP Modulation and Hybrid Post Equalizer," *IEEE Photonics Journal,* vol. 7, no. 6, pp. 904-

907, 2015.

[23] F. Zafar, M. Bakaul and R. Parthiban, "Laser-diode-based visible light communication: Toward gigabit class communication," *IEEE Communications Magazine,* vol. 55, no. 2, pp. 144-151, 2017.

[24] M. S. Islim and all, "Towards 10 Gb/s orthogonal frequency division multiplexing-based visible light communication using a GaN violet micro-LED," *Photonics Research,* vol. 5, no. 2, pp. A35-A43 , 2017.

[25] Y. Chi and all, "Phosphorous Diffuser Diverged Blue Laser Diode for Indoor Lighting and Communication," *Scientific Reports,* vol. 5, pp. 1-9, 2015.

[26] Islam, R; Choudhury, P; Islam, M A;, "Analysis of DCO-OFDM and flip-OFDM for IM/DD optical-wireless system," in *8th International Conference on Electrical and Computer Engineering*, Dhaka, 2014.

[27] A. Gomez, K. Shi, C. Quintana and all, "Design and Demonstration of a 400 Gb/s Indoor Optical Wireless Communications Link," *IEEE Journal of Lightwave Technology,* no. 99, pp. 1-8, 2016.

[28] A. Gomez, K. Shi, C. Quintana and all, "Beyond 100-Gb / s Indoor Wide Field-of-View Optical Wireless Communications," *IEEE Photonics Technology Letters,* vol. 27, no. 4, pp. 367-370, 2015.

[29] A. Gomez, K. Shi, C. Quintana and all, "A 50 Gb / s Transparent Indoor Optical Wireless Communications Link with an Integrated Localization and Tracking System," *IEEE Journal of Lightwave Technology,* vol. 34, no. 10, pp. 1-8, 2016.

[30] K. Wang, S. Member, A. Nirmalathas and all, "4 x 12 . 5 Gb / s WDM Optical Wireless Communication System for Indoor Applications," *IEEE Journal of Lightwave Technology,* vol. 29, no. 13, pp. 1988-1996, 2011.

[31] C. W. Oh, F. M. Huijskens, S. Zou and all, "36.7 Gbps Spectrum-efficient Indoor Optical Wireless System with Beam-Steering," in *ECOC*, 2014.

[32] J. Wang, J. Yang, I. M. Fazal and all, "Terabit free-space data transmission employing orbital angular momentum multiplexing," *Nature Photonics,* vol. 6, 2012.

[33] H. Huang, G. Xie, Y. Yan and all, "100 Tbit/s free-space data link enabled by three-dimensional multiplexing of orbital angular momentum, polarization, and wavelength," *Optics Letter,* vol. 39, no. 2, pp. 197-200, 2014.

[34] E. Ciaramella, Y. Arimoto, G. Contestabile and all, "1.28 Terabit/s (32x40 Gbit/s) WDM Transmission System for Free Space Optical Communications," *IEEE Journal on Selected Areas in Communications,* vol. 27, no. 9, pp. 1639-1645, 2009.

[35] Z. Ghassemlooy, "2 x 80 Gbit/s DWDM Bidirectional Wavelength Reuse Optical Wireless Transmission," *IEEE Photonics Journal,* vol. 5, no. 4, p. 7901708–7901708, 2013.

[36] V. C. (US). [Online]. Available: https://store.steampowered.com/steamvr#HowItWorks.

[37] Virtual Reality Society, "History Of Virtual Reality," 2016. [Online]. Available: https://www.vrs.org.uk/virtual-reality/history.html.

[38] P. Fuchs, G. Moreau and P. Guitton, Virtual Reality: Concepts and Technologies, CRC Press, 2011.

[39] K. Rolf, M. Brzozowski and S. Nowak, "Reliable architecture for heterogeneous home-networks: The OMEGA I-MAC approach.," in *Telecommunication in Modern Satellite Cable and Broadcasting Services (TELSIKS)*, 2011.

[40] J. Guerreiro, R. Dinis and P. Montezuma, "On the impact of the clipping techniques on the performance of optical OFDM," in *5th International Conference on Optical Communication Systems (OPTICS)*, Vienna, 2014.

[41] D. O'Brien and all, "High-speed optical wireless demonstrators: Conclusions and future directions," *Journal of Lightwave Technology,* vol. 30, no. 13, pp. 2181-2187 , 2012.

[42] C. W. Oh, E. Tangdiongga and A. M. J. Koonen, "Steerable pencil beams for multi-Gbps indoor optical wireless communication," *Optics Letters,* vol. 39, no. 18, pp. 5427-5430, 2014.

9 Appendix A1

Figure 59 to Figure 61 show the BER performance versus SNR for different FEC coding schemes of different information block lengths (*K*) adopting range of code rates (*R*). These results depict that turbo, LDPC and polar codes perform close to each other, which is the more true the larger the information block length (*K*).

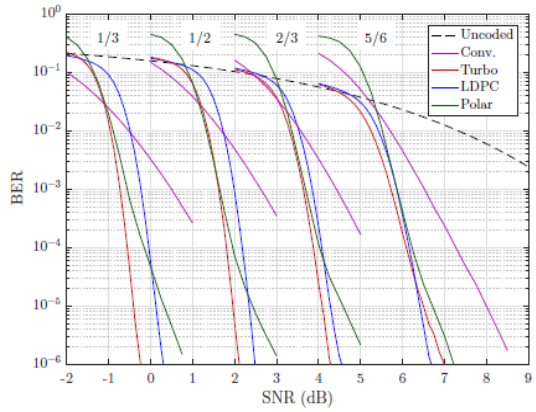


Figure 59 - BER comparison for different code rates, K= 512 (For LDPC, K= 516 for R= 1/2, and 1/3, and K= 520 for R= 5/6.)

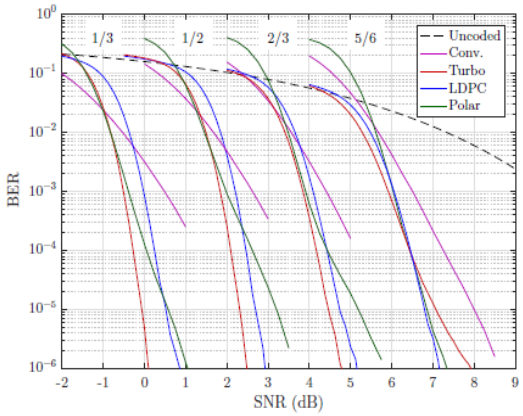


Figure 60 - BER comparison for different code rates, K= 1024 (For LDPC, K= 1020 for R= 1/2, 1/3, and 5/6.)

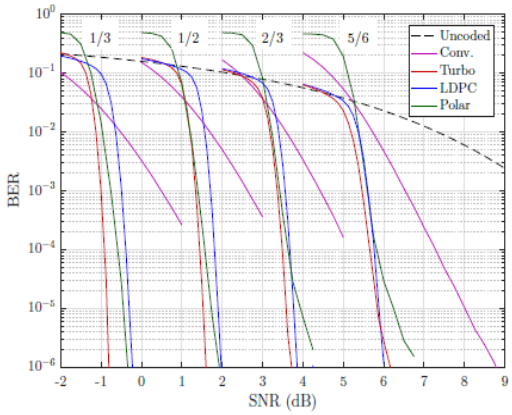


Figure 61 - BER comparison for different code rates, K= 8192 (For LDPC, K= 8196 for R= 1/2, and 1/3, and K =8200 for R =5/6.)

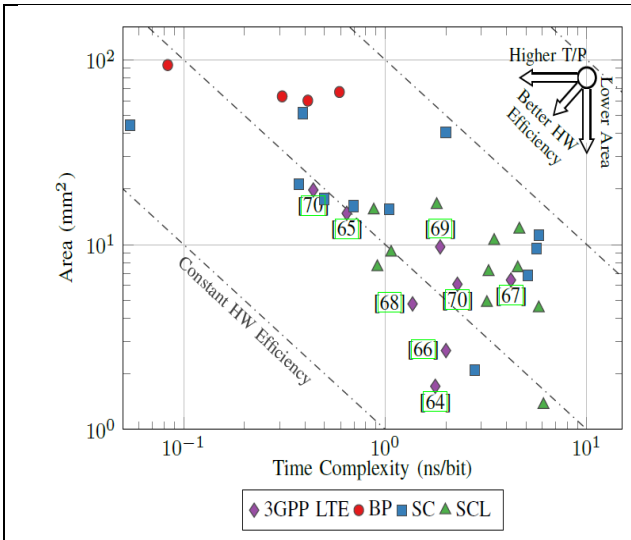


Figure 62 - Hardware efficiency of 3GPP LTE Turbo decoders against that of polar decoders

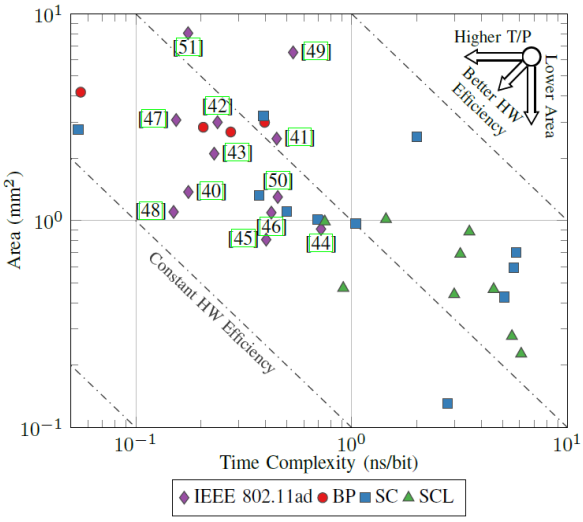


Figure 63 - Hardware efficiency of IEEE 802.11 ad decoders against that of polar decoder

In Figure 62, it is observed that, on average, the LTE Turbo decoders have similar hardware efficiency to the polar decoders. Moreover, it is noticed that polar BP decoders match the throughput of Turbo decoder at the cost of higher HW complexity. From Figure 63, it can be seen that, on average, IEEE 802.11ad LDPC decoders have slightly higher hardware efficiency against polar BP decoders. While the hardware efficiency of polar SCL decoders is similar to LDPC decoders due to their lower area requirements, most SCL decoders have lower throughput. Based on the results shown, the table below summarizes the comparison of FEC schemes in terms of above-mentioned performance metrics.

10 Appendix A2

AFE schematic diagrams

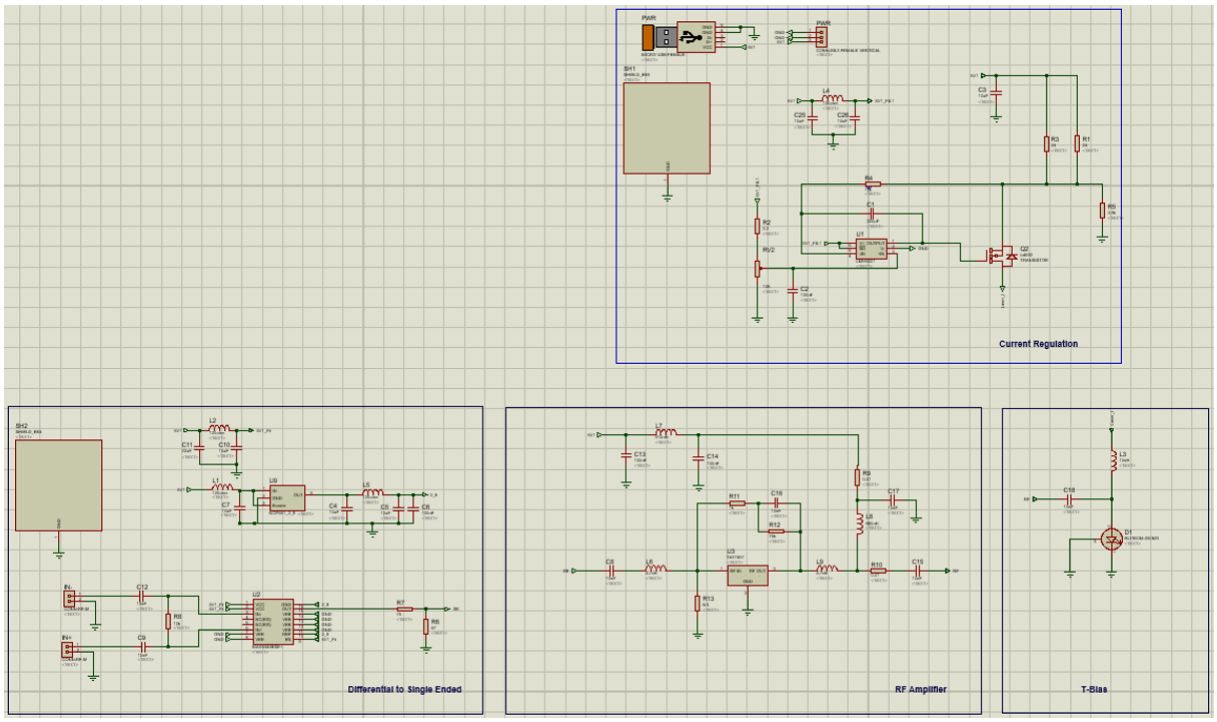


Figure 64 - AFE Tx schematic

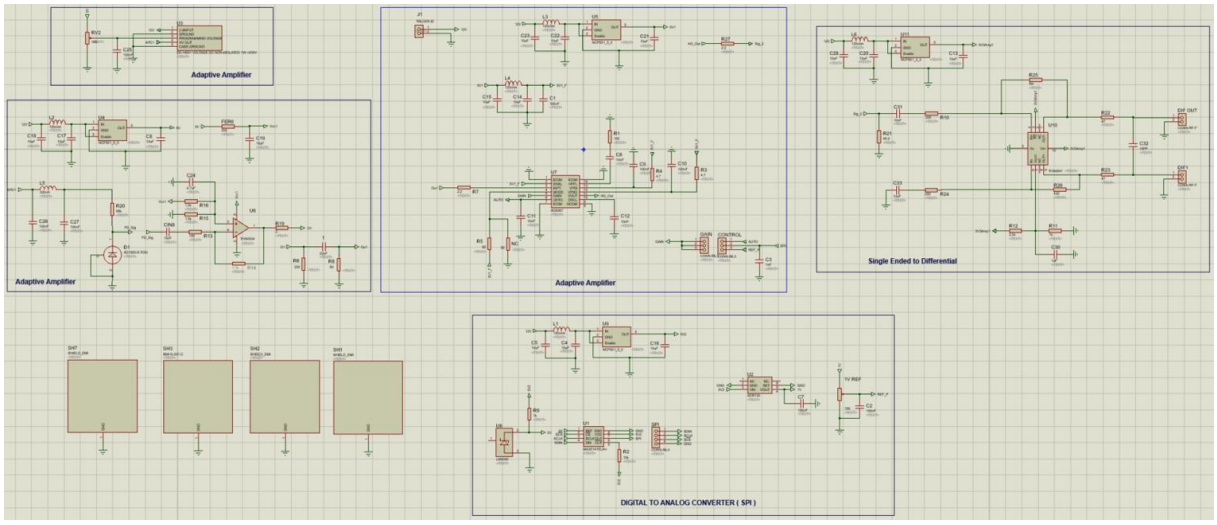


Figure 65 - AFE RX schematic