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Optical Wireless Communications and radio prototypes test results

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Abstract

This deliverable presents WORTECS overall Proof of Concept (PoC), Optical Wireless Communication (OWC) provides by Oledcomm (OLD) and pureLiFi (PLF), Fibre Wireless Fiber proposes by University of Oxford (OXF) and Radio Frequency (RF) link defines by IHP (IHP). These different links are managed by Heterogeneous Network (HetNet) board achieved by IHP. Virtual Reality (VR) or Mixed Reality (MR) use case will be shown with the help of Video Converter (VC) board and Virtual Reality content from B<>COM (BCM). Propagation model first results will be also proposed by university of Las Palmas (ULP).
The main issue of this document is to define the PoC main features and present prototypes V1 test results.

Keyword list
Optical wireless transmission, radio transmission, mutualisation, reconfigurable, Fibre Wireless Fibre (FWF), FiWi (Fibre Wireless), Heterogeneous Networks (HetNet), Test Results

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List of Acronyms

Acronym	Meaning
ACO-OFDM	Asymmetrically Clipped Optical OFDM
ADC	Analog to Digital Converter
A/D	Analog to Digital
AFE	Analog Front End
APD	Avalanche Photodiode
ASIC	Application-Specific Integrated Circuit
AWG	Additive White Gaussian
AWGN	Additive White Gaussian Noise
BER	Bit Error Rate
BP	Believe Propagation
CP	Cyclic Prefix
CIR	Channel Impulse Response
CFO	Carrier Frequency Offset
dB	Decibel
D/A	Digital to Analog
DAC	Digital-to-Analog Converter
DC	Direct Current
DCO-OFDM	DC biased Optical OFDM
DFT	Discrete Fourier Transform
DVB	Digital Video Broadcasting
EIRP	Effective Isotropic Radiated Power
FEC	Forward Error Code
FFC	Free-From Optical Concentrator
FFT	Fast Fourier Transform
FIR	Finite Impulse Response
FiWi	Fibre Wireless
FBMC	Filter-Bank Multicarrier
FOV	Field of View
FPGA	Field Programmable Gate Array
FWF	Fiber Wireless Fiber
FWHM	Full Width at Half Maximum
Gbps	Giga bits per second
GND	Ground
HMD	Head Mounted Display
HSPA	High Speed Packet Access
IFFT	Inverse Fast Fourier Transform
IM/DD	Intensity Modulation / Direct Detection
IR	Infra-Red
ISI	Inter Symbol Interference
LDPC	Low Density Parity Check
LED	Light-Emitting Diode
LO	Local Oscillator
LOS	Line Of Sight
LTE	Long Term Evolution
MAC	Medium Access Control

MCRT	**Monte Carlo Ray Tracing**
MCS	**Modulation and Coding Scheme**
MIMO	**Multiple-Input Multiple-Output**
NIR	**Near Infra-Red**
NLOS	**Non Line Of Sight**
OFDM	**Orthogonal Frequency Division Multiplex**
OFDM-MConst	**OFDM with multiple constellations**
OFE	**Optical Front End**
OOB	**Out Of the Band**
O-OFDM	**Optical OFDM**
ODH	**Optical Detector Head**
OTH	**Optical Transmission Head**
OWC	**Optical Wireless Communication**
PA	**Power Amplifier**
PAM- DMT	**Pulse-Amplitude-Modulated Discrete-Multitone**
PAPR	**Peak-to-Average Power Ratio**
PCB	**Printed Circuit Board**
PCC	**Parabolic Compound Concentrator**
PHy	**Physical layer**
PRBS	**Pseudo-Random Binary Sequence**
P/S	**Parallel to Serial**
QC-LDPC	**Quasi-Cyclic LDPC**
RF	**Radio Frequency**
RMS	**Root Mean Square**
SC	**Single Carrier or Successive-Cancellation**
SCL	**Successive-Cancellation List**
SISO	**Single Input Single Output**
SNR	**Signal to Noise Ratio**
S/P	**Serial to Parallel**
SP	**Sum-Product**
SPI	**Serial Peripheral Interface**
TIR	**Total Internal Reflections**
UFMC	**Universal Filtered Multi-Carrier**
VC	**Video Converter**
VGA	**Variable Gain Amplifier**
VR	**Virtual Reality**
WORTECS	**Wireless Optical/Radio TErabit CommunicationS**
ZP	**Zero Prefix**

Table of contents

1 Introduction 8

2 Optical Wireless Communication PoC 9

2.1 Features 9
2.1.1 Optic and Analog Board (OLD) 9
2.1.2 Digital board (PLF) 11

2.2 Test results 12

3 Fibre Wireless Fiber PoC 16

3.1 Features 16

3.2 Testing and performance results 18
3.2.1 Pointing loss 18
3.2.2 Tracking system accuracy 18
3.2.3 Transmission losses and tracking 19
3.2.4 Link operation and Coverage 20

4 Radio link PoC 24

4.1 Features of the RF wireless link 24

4.2 Test results 25
4.2.1 Throughput measurement 25
4.2.2 Latency measurement 26
4.2.3 Conclusion 27

5 Heterogeneous Network PoC 28

5.1 Features 28

5.2 Test results 29
5.2.1 Throughput 29
5.2.2 Other 29

6 Video Converter PoC 31

6.1 Features 31

6.2 Test results 33
6.2.1 Latency 33
6.2.2 Compression ratio and Throughput 33
6.2.3 Packet loss or error 34

7 Propagation model 35

7.1 Use of Gaussians as emission patterns 35

7.2 Standalone software development 36

7.3 Contributions to 802.11bb standard 37

8 PoC V1 overall result and conclusion 38

9 References 40

List of Tables

Table 1: FWF Demonstrator Notation and Parameters 16
Table 2: System features and specification 17
Table 3 - iperf3 throughput tests 26
Table 4 – Video converter compression rate 34

List of Figures

Figure 1 - WORTECS PoC V1 demonstrator 8
Figure 2: OWC high level block diagram 9
Figure 3 - OFE board architecture and interface description. 9
Figure 4 - (a) Bottom and (b) top view of the OFE board with the description of the interfaces and without the receiving optics. 10
Figure 5 - High-bandwidth APD receiver Thorlabs APD430A2 used as reference receiver. 10
Figure 6: FPGA based OWC baseband architecture 11
Figure 7: PLC based OWC baseband 12
Figure 8: Frequency response of the custom-made OWC (a) transmitter and (b) receiver. 12
Figure 9: Frequency response of the OWC reference receiver (Thorlabs APD430A2). 13
Figure 10: FPGA based OWC PHY test configuration 13
Figure 11: FPGA based OWC PHY set-up 14
Figure 12: PLC based OWC test configuration 14
Figure 13: PLC based OWC PHY test set-up 15
Figure 14: SNR vs. PER for the PLC based solution 15
Figure 15: Block diagram of FWF system 16
Figure 16: Assembled transmitter (left) and receiver (right) units. 17
Figure 17: Additional loss (dB) due to pointing misalignment. Left hand figure shows transmitter pointing, receiver static. Right hand figure shows receiver pointing, transmitter static. 18
Figure 18: The accuracy of the coarse tracking cameras. 18
Figure 19: The accuracy of the fine tracking cameras. 19
Figure 20: Received power vs transmitter rotation and steering in horizontal and vertical planes. 19
Figure 21: Received power vs receiver rotation and steering in horizontal and vertical planes. 20
Figure 22: BER performance of FTLX1871M3BCL SFP+ module for a 10.3 Gbit/s free-space transmission. 20
Figure 23: Bore sight communication range of FWF terminals with SFP+ based 10.3 Gbit/s free-space transmission. 21
Figure 24: FWF terminal setup in 4 x 4 x 3 meter indoor testing facility at BCOM laboratory. The AP terminal in one corner at 3.5m height (left), the UE terminal on the room floor (centre) and VR-HMD connected to the UE terminal (right). 22
Figure 25: FWF terminal down-link (top) and up-link (bottom) received power levels (dBm) for 10.3 Gbit/s free-space transmission when the UE terminal moved across the room floor. 23
Figure 26 - Test setup for testing of the 60 GHz RF link 24
Figure 27 - Photo of the test setup 25
Figure 28 - Latency distribution mesured with ping command 26
Figure 29 - Measurement of the latency using the HDMI - Ethernet converter 27
Figure 30 Heterogenous Network are support by our FPGA-based switches that implement the new Laye2.5 28
Figure 31 The HetNet switch, which implements the Layer2.5, switch the current link to another (handover), for instance, on problems with the current connection 29
Figure 32 Test setup used to examine the throughput of the Layer2.5 29
Figure 33 - Function distribution 31
Figure 34 - Hardware integration 32
Figure 35 - User and server video converter configuration for test 32
Figure 36 - Video converter modules latency 33
Figure 37: Error probability associated to rejecting the null hypothesis (p-value) of assuming Generalized Lambertian statistically equal to a Normal distribution. 36
Figure 38: Proposed architecture for WORTECS' standalone CIR simulator 36
Figure 37 - WORTECS PoC V1 results 38
Figure 38 - WORTECS PoC V2 targets 39

1 Introduction

The main objective of this deliverable focuses on the Proof of Concept (PoC) new communication systems based on high frequency radio (> 90 GHz) and optical wireless communications for multi-Gigabits transmission. The cooperation/aggregation between different Radio and optical Wireless Access Technologies (WAT), leading to the design of a specific Hybrid Networks architecture (Heterogeneous Network), will allow these to achieve Terabit transmission rates. The main issues to be addressed are to show the PoCs features and compare them with test results in terms of throughput, latency, positioning, capacity, coverage.

This deliverable is divided into several parts. Each parts containing specific PoC or propagation model, described in main features following by test results. The last past show the global WORTECS demonstrator V1 with the different prototypes integrated in virtual reality processing chain content as define on Figure1.

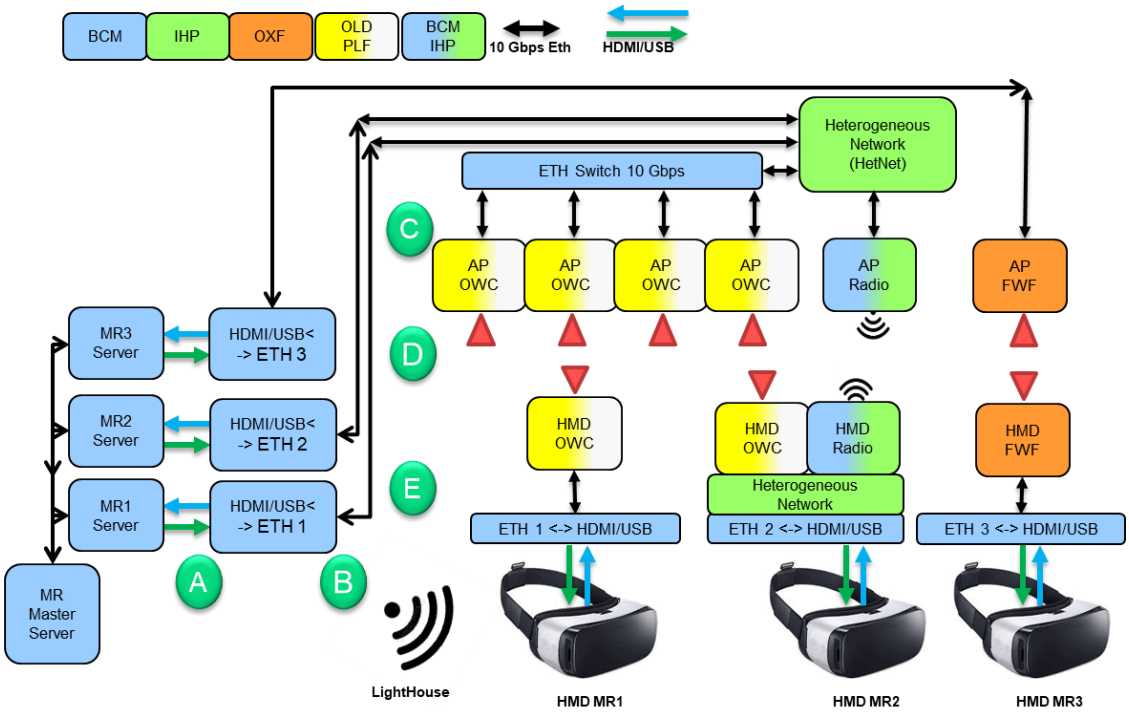


Figure 1 - WORTECS PoC V1 demonstrator

More precisely, for the first WORTECS demonstrator version, partners targeted:

- Developed Optical Wireless Communication (OWC) systems design offering multi Gbps rates in room (yellow and white box/OLD and PLF).
- Developed novel (infrared) optical steering systems with Fiber Wireless Fiber (FWF) design to deliver ultra-high data rate (up to 10 Gbps for the PoC V1) for point to point links (Orange box/OXF).
- Developed radio mm-wave prototype design links operating at 60 GHz, able to deliver up to 4 Gbps with low latency (Blue and Green box/IHP and BCM).
- Developed network coordination systems (HetNet) in order to deliver ultra-high data rate, with low latency, in a multi Wireless Access Technologies (WAT) environment, i.e. Radio and OWCs for the PoC V1 (Green box/IHP).
- Developed Video Converter (VC = HDMI and USB ports to Ethernet port) prototype able to work at ultra-high data rate with tuneable compression ratio (Blue box/BCM).
- Developed an ultra-high data rate video content “Artic Sea” for Mixed Reality V1 use case (Blue box/BCM).

2 Optical Wireless Communication PoC

WORTECS demonstration scenario is characterized in [1].

2.1 Features

The OWC PoC is developed by partners OLED and PLF. PLF is responsible for the 1Gbps capable PHY layer including the analogue to digital (A/D), digital to analogue (D/A) and the 10G Ethernet interfaces. OLED is responsible to develop the analogue front-end, including the analogue circuitry, the optoelectronics and optical components that are capable of transmitting the required 1Gbps data rate. Figure 2 shows the distribution of tasks between OLED and PLF.

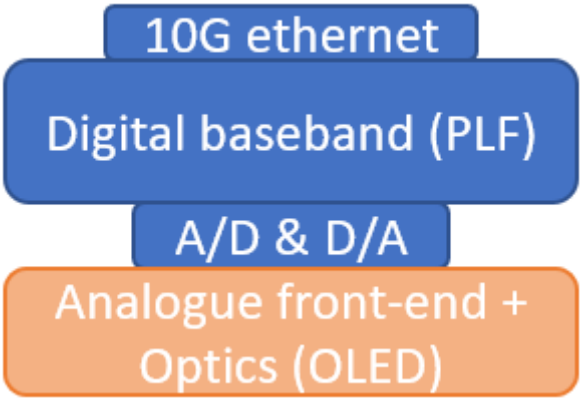


Figure 2: OWC high level block diagram

2.1.1 Optic and Analog Board (OLD)

The OFE architecture is represented on figure 3. It is composed of two main channels: the transmission channel and the reception channel.

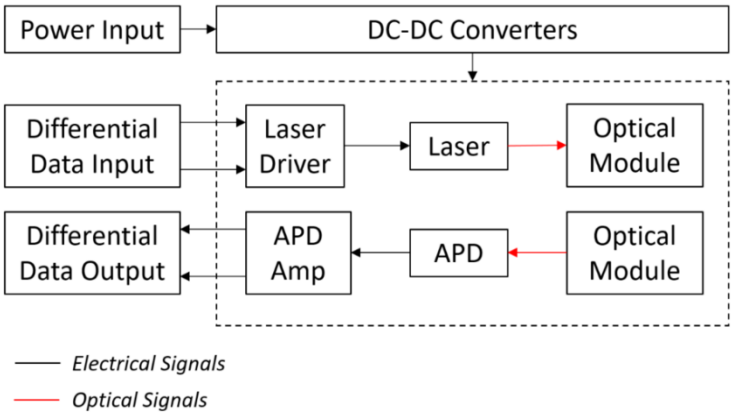


Figure 3 - OFE board architecture and interface description.

In a first version, the transmission channel is composed of:

- A laser driver with differential inputs for interfacing with PLF baseband,
- A vertical-cavity surface-emitting laser (VCSEL) (Ref: OSRAM PLPVQ 940A), which already integrates an optical diffuser.

The reception channel is composed of:

- A custom-made concentrator of designed FOV 30°,
- A avalanche photodiode (APD, Ref: First Sensor AD1900-8 TO),
- An APD amplifier with differential outputs for interfacing with PLF baseband.

All these components are embedded on a single electronic board, represented on Figure 4, along with the power supply stages and interfacing connectors.

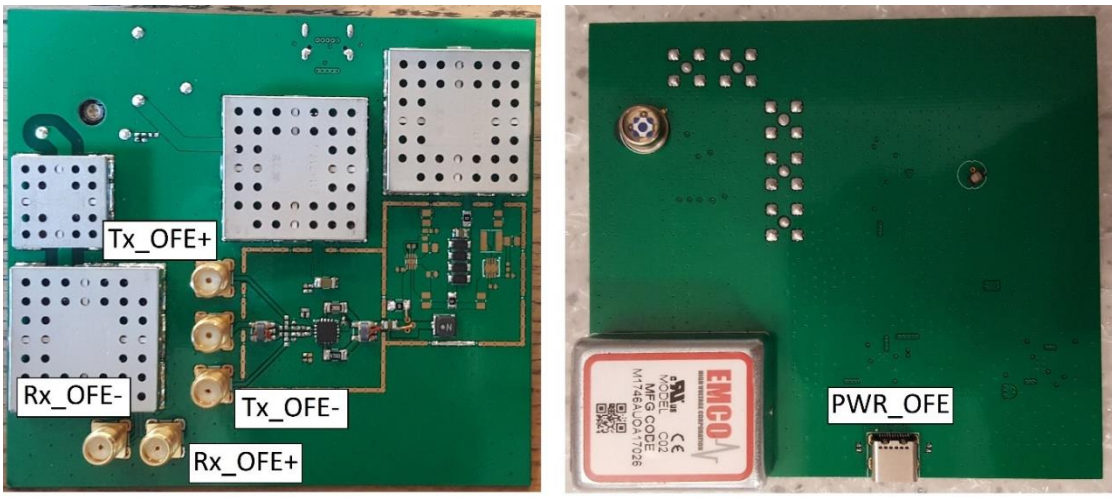


Figure 4 - (a) Bottom and (b) top view of the OFE board with the description of the interfaces and without the receiving optics.

A Thorlabs APD430A2, represented on Figure 5, is also used as a reference receiver providing sufficient bandwidth to reach a 1Gbps data transmission but with a limited sensitive surface which will necessarily limit the communication range.

Figure 5 - High-bandwidth APD receiver Thorlabs APD430A2 used as reference receiver.

2.1.2 Digital board (PLF)

PLF has initially developed a proprietary baseband solution, implemented on the Xilinx ZCU111 SoC platform. The design utilizes the R5 real time processors, the FPGA fabric RF DAC and ADC functionality on the XCZU28DR-2FFVG1517 SoC.
The following figure shows the baseband architecture implemented.

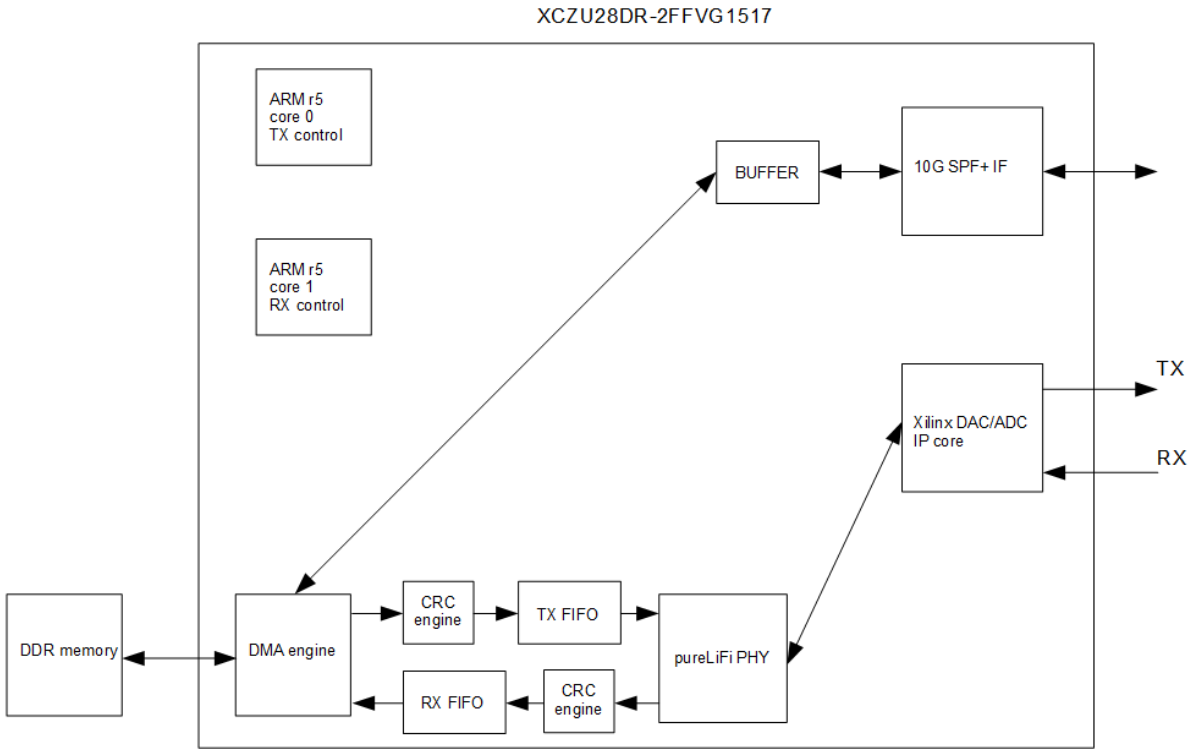


Figure 6: FPGA based OWC baseband architecture

The following list details the features of the designed and implemented system:

- Development of proprietary LiFi PHY with the following features
  - 1024 pt FFT
  - Adaptive bit-loading
  - 802.11 BCC channel coding
  - Serial transmission of real and imaginary parts of the signal, in order to convert the complex OFDM signal into real.
  - Optimized packet structure for minimum overhead.
  - Implementation of PN sequences…
  - Transmission of header data over pilot tones.
  - Pipelining in order to minimize packet interspacing. The receiver is able to accept the arriving packets while it is busy decoding the previous packet.
- Design of the 10G SFP+ interface
  - For the PHY, the free Xilinx IP core has been used.
  - An open source MAC is used, taken from opencores.org
  - Buffer management has been designed
- System integration
- Software development for the r5 processors
  - pureLiFi MAC protocol
  - Packet aggregation to improve efficiency

In parallel to the baseband implementation on the Xilinx platforms, an alternative solution has been considered due to the high cost and change in the direction of 802.11bb standard. This solution reuses an off-the-shelf PLC (powerline communication). The designed board is shown in Figure 7.

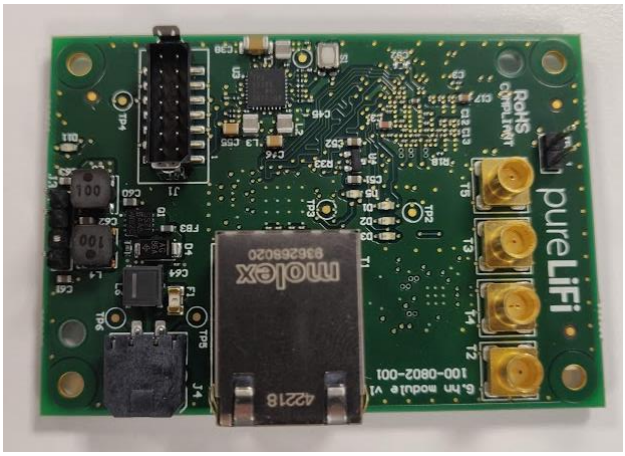


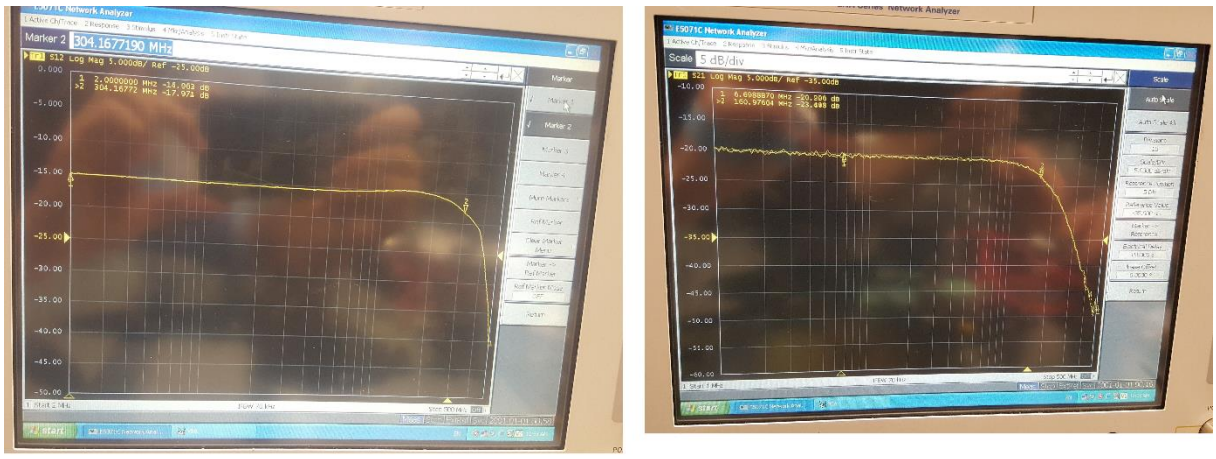
Figure 7: PLC based OWC baseband

2.2 Test results

2.2.1 OFE characterization

In order to reach a communication data rate at a given distance, the OFE must provide and overall bandwidth of 200MHz with the PLC baseband and 250MHz with the FPGA baseband, along with a signal-to-noise ratio (SNR) of 25dB.

Figure 8(a) shows the frequency response of the custom-made OWC transmitter represented on Figure 4. It shows that the 3dB modulation bandwidth reaches 304 MHz, which is larger than the requirements for both the PLC and FPGA basebands. On the other hand, Figure 8(b) shows the frequency response of the custom-made OWC receiver. We can see that the 3dB bandwidth reaches this time 160 MHz, which is below the requirements for both the PLC and FPGA baseband solutions.



(a) **(b)**

Figure 8: Frequency response of the custom-made OWC (a) transmitter and (b) receiver.

Preliminary tests with these custom made transmitter and receiver along with the PLC baseband showed that the data rate at 2 cm is around 650 Mbps. This data rate limitation comes from the insufficient bandwidth of the custom made receiver.

As a comparison, the frequency response of the reference photoreceiver is represented in Figure 9. It appears clearly that the receiver bandwidth is larger than 350MHz, whatever the gain, which should be sufficient to reach the targeted data rate, despite a limited sensitive surface which will limit the commuication range. Therefore, the rest of the tests have been carried out with the reference receiver rather than with the custom-made receiver, which will be improved in future developments.

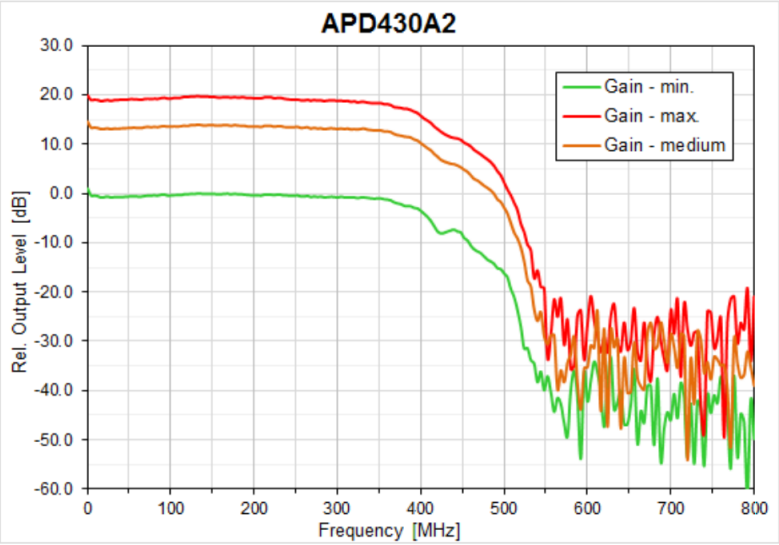


Figure 9: Frequency response of the OWC reference receiver (Thorlabs APD430A2).

2.2.2 FPGA-based solution

Two of the FPGA boards were used to test an end-to-end connection. Figure 10 and Figure 11 show the test-setup used to test the system.

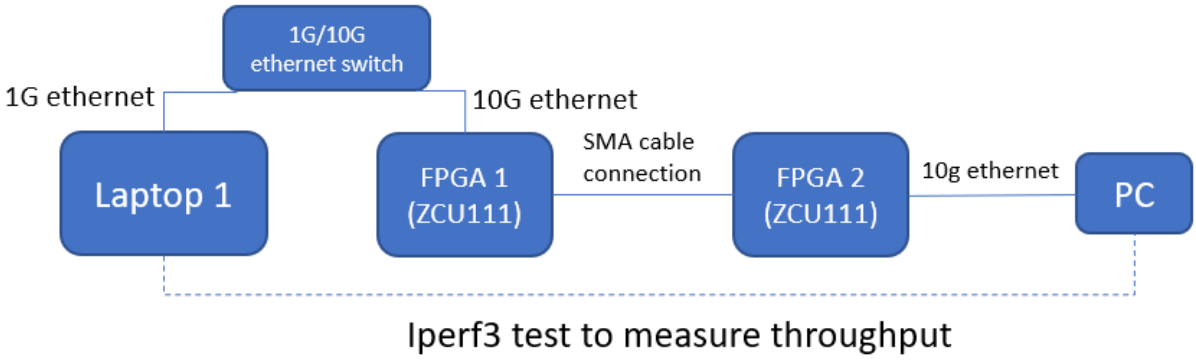


Figure 10: FPGA based OWC PHY test configuration

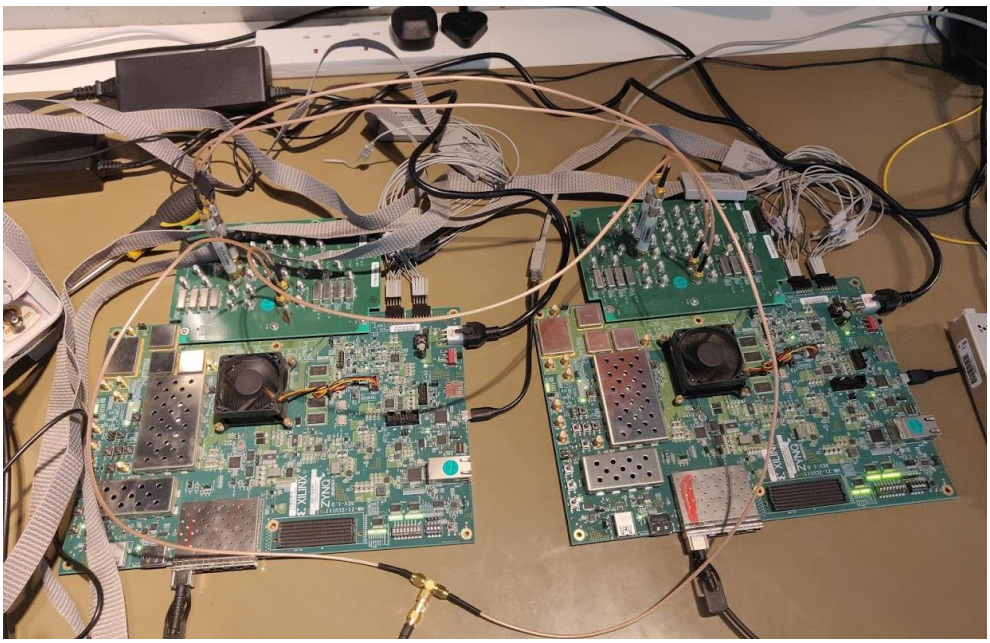


Figure 11: FPGA based OWC PHY set-up

The following performance was measured with this set-up:

- 900 Mbps UDP throughput
- 0% packet loss
- <1ms latency from AP to STA

The integration of the baseband boards with BCOM video server was unsuccesful. At system start-up packet loss was observed which the video server was not able to tolerate. To succesfuly integrate the system this initial packet loss and the video server sensitivity to packet loss shall be addressed.

2.2.3 PLC based solution

Two PLC boards (PLF) with an optical downlink (OLED) and a cabled uplink connection were used to measure the system performance. The optical link consisted of a transmitter designed by OLED and an off the shelf reference receiver. Figure 12 and 13 show the configuration and the set-up that was used to test the system.

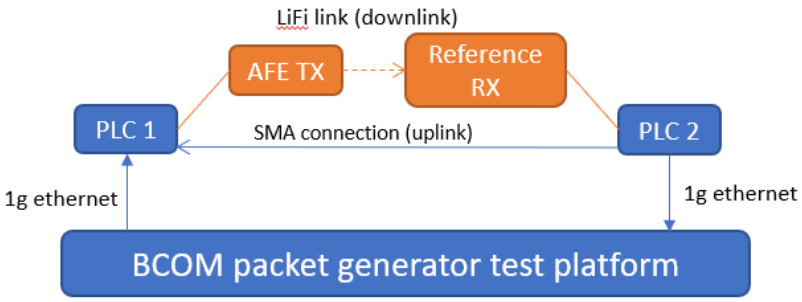


Figure 12: PLC based OWC test configuration

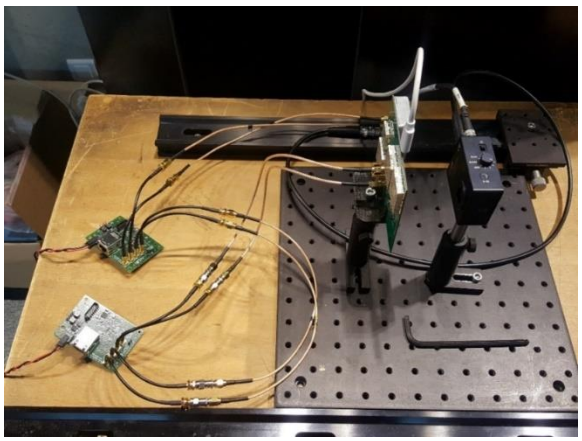


Figure 13: PLC based OWC PHY test set-up

Instead of iperf, a more representative test was used to determine the link performance. BCOM has provided a packet generator to emulate a VR like data flow. This tool was designed to measure packet-loss and latency when a VR-like packet flow of 800Mbps is transmitted. The following results were obtained at a <10cm distance between the TX and the RX:

- PER << 1%
- Latency < 2ms

The variation of PER with SNR is shown in Figure 14. To control the SNR the transmitter angle was varied. This measurement gives an indication on the SNR required to sustain a given PER. It can be seen that to sustain a PER of 1%, a link SNR of ~24dB is required.

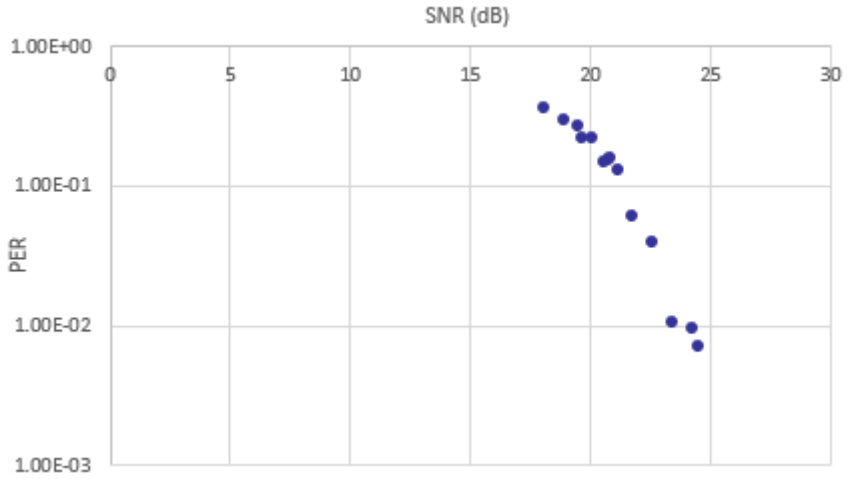


Figure 14: SNR vs. PER for the PLC based solution

3 Fibre Wireless Fiber PoC

This section introduces the FWF system, its current features and test results.

3.1 Features

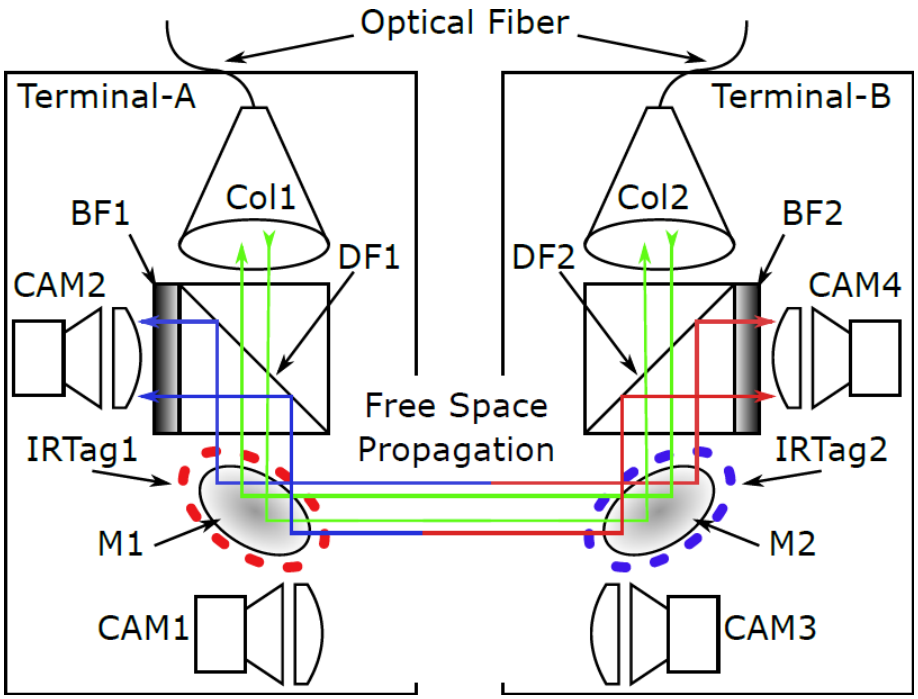


Figure 15: Block diagram of FWF system

Figure 15 shows the demonstrator architecture and Figure 16 shows the assembled units. Some parametric and notational details are shown in Table 1. Figure 15 shows that this is a co-design of a narrow-beam optical wireless communication system and an optical localisation and tracking system. More information on the state-of-the-art (SoTA) FWF systems can be found in D3.1.

The green lines shown in Figure 15 represent a narrow 1550 nm beam of light, which carries the communication information. This is light from an optical fiber based transmitter, which is connected to terminal A via an optical fiber. This light is collimated at Terminal-A, and steered towards Terminal-B with the use of a dual-axis mirror from OptoTune. The OptoTune mirror provides ±25° mechanical tilt, resulting in ±50° optical deflection. At Terminal-B, another OptoTune mirror steers the beam towards the collimator, which focuses the beam and launches it back into the optical fiber. A optical fiber based receiver then decodes the optical signal.

Table 1: FWF Demonstrator Notation and Parameters

Notation	Details
BF1	Bandpass Filter-1, Central Wavelength 800 nm
BF2	Bandpass Filter-2, Central Wavelength 900 nm
Col1, Col2	Collimator-1 and Collimator-2
CAM1, CAM3	PixyCams with 50° horizontal and 30° vertical half Field-of-View (FoV)
CAM2, CAM4	PixyCams with 4° horizontal and 2.2° vertical half Field-of-View (FoV)
DF1,DF2	Dichroic Filter 1 and 2, cut-off at 900 nm

IRTag1	890 nm Infrared beacon for tracking
IRTag2	800 nm Infrared beacon for tracking
M1, M2	OptoTune mirrors for beam-steering

In order to steer the optical beam from Terminal-A to Terminal-B, and vice-versa, accurate location information of the opposite terminal is required. Therefore, a localisation and tracking system is required. As detailed in D3.1 and as shown in Figure 15, digital tracking cameras (pixycam) based localisation and tracking system has been developed. On each terminal there is a wide FoV camera (CAM1 at Terminal-A and CAM3 at Terminal-B) which is used to locate the IRTag on the opposite terminal with low resolution. The mirror is then steered to the appropriate direction. A fine-tracking camera with narrow FoV (CAM2 and CAM4 on A and B respectively) is placed on the terminal so the centre of its FoV tracks with the angular position of the steering mirror, and this is then used to locate the IRTag on the opposite terminal. The mirror is then steered once more, so that the Tag centre is centred on the fine-tracking camera. In practice calibration is required to account for alignment offsets of the tracking system with the communications system. The IRTags are circular rings formed by infrared LEDs, with a central wavelength of 800 nm and 890 nm for each terminal. The BF1 and BF2 optical filters prevent interference between the tracking systems at each terminal while DF1 and DF2 prevent interference between the communication and tracking links.

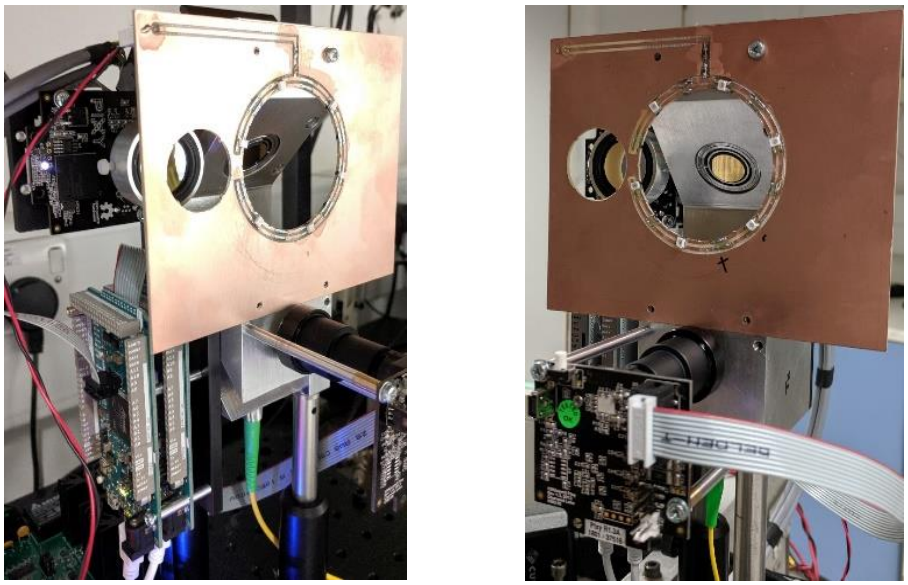


Figure 16: Assembled transmitter (left) and receiver (right) units.

The characteristics of the system are shown in Table 2.

Table 2: System features and specification

Operating Field of View	+/- 25 degrees horizontally and vertically
Tracking system resolution (theoretical)	0.014 degrees horizontally and Vertically (corresponding to 1 camera pixel)
Tracking system resolution (measured)	0.021 degrees horizontally and 0.014 degrees Vertically (corresponding to 1 camera pixel)
Communications wavelength	1300-1600 nm (bidirectional)
Fibre input/output	SMF 28- APC connectors
Free space beam diameter	1.12 mm (theoretical) at Collimator output
Transmission power	Limited to <7dBm (Class 1 operation) by control of laser power
Tracking beacon wavelength	800 nm terminal A and 890 nm terminal B

3.2 Testing and performance results

3.2.1 Pointing loss

Tests were undertaken to ascertain the required pointing and tracking accuracy. Figure 17 shows tests when the transmitter is pointed at a static receiver, and the receiver pointed at a static transmitter. It can be seen that a +/- 0.01 degree misalignment in pointing results in an additional loss of approximately 3dB relative to maximum transmission. The tracking system was designed keeping this additional misalignment loss in mind.

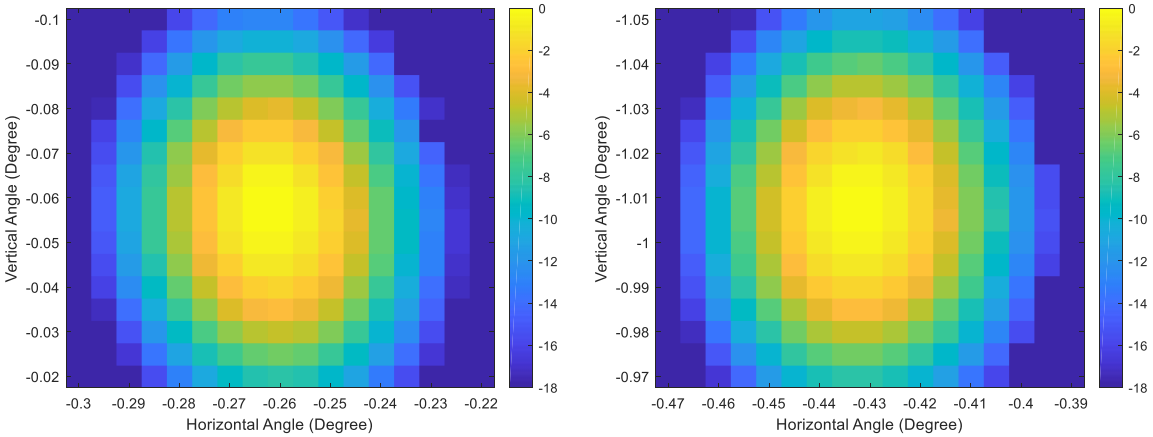


Figure 17: Additional loss (dB) due to pointing misalignment. Left hand figure shows transmitter pointing, receiver static. Right hand figure shows receiver pointing, transmitter static.

3.2.2 Tracking system accuracy

Figure 18 and 19 show the tracking accuracy of the coarse and fine tracking cameras, respectively. These results are obtained by mounting the cameras on a rotation stage placed at 5m distance from the IR tag. The results show that the coarse tracking error remains below 1° in horizontal plane and below 0.6° in the vertical plane. Similarly, the fine tracking error remains below 0.015° for most of the horizontal and vertical FoV.

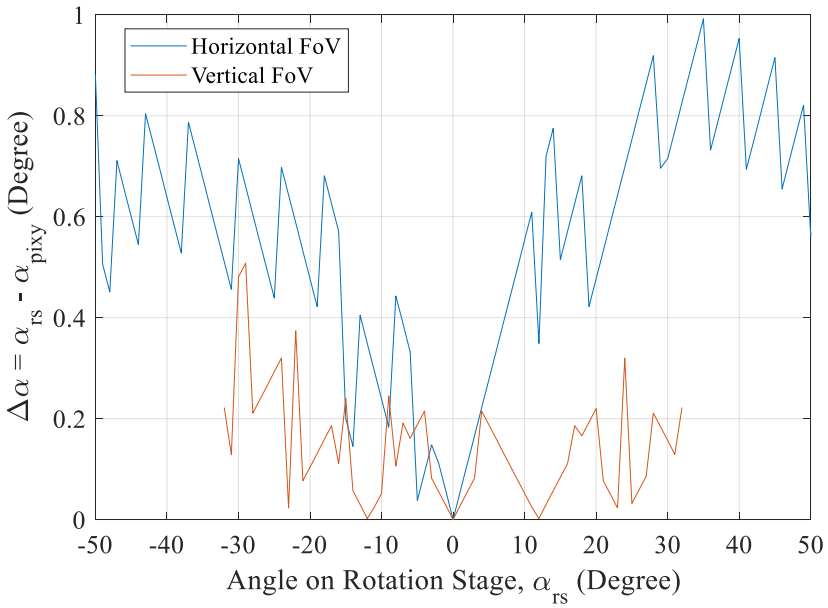


Figure 18: The accuracy of the coarse tracking cameras.

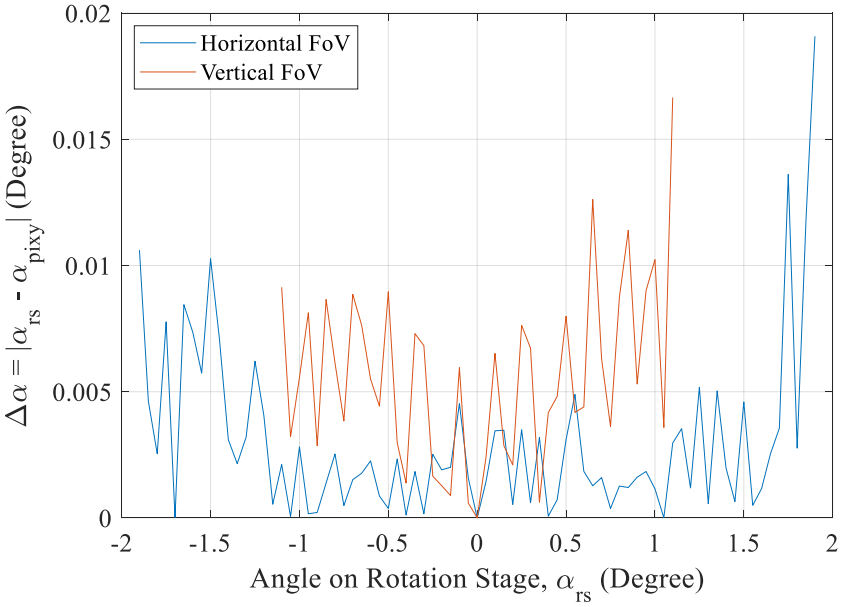


Figure 19: The accuracy of the fine tracking cameras.

3.2.3 Transmission losses and tracking

Link-loss (optical power loss) experiments were undertaken to determine the performance of the FWF terminals. The terminals were placed at a distance of 3.5m from each other. One of the terminals was rotated using a rotation stage. Then localization and beam steering was performed to align the system and power at the receiver side was measured. The communications link was provided by a Class 1 SFP+ transceiver operating at 10Gbps, which was plugged into a bit error ratio tester (BERT). The output power of the SFP+ transceiver is 0 dBm and the receiver sensitivity is -27 dBm, giving link budget of 27 dB.

Figures 20 and 21 show the received power level with link angle for transmitter and receiver rotation, respectively. The results show that the link-loss when terminals are at bore sight is 7 dB. Overall, the link-loss per terminal is less than 10 dB for a FoV of less than +/-20 degrees. Given the boresight loss is ~7dB an additional 3-5 dB loss can be attributed to tracking. Therefore, for a rotation in either horizontal or vertical plane, the net link-loss for both transmitter and receiver should remain below 20 dB approximately, which is within the available link budget.

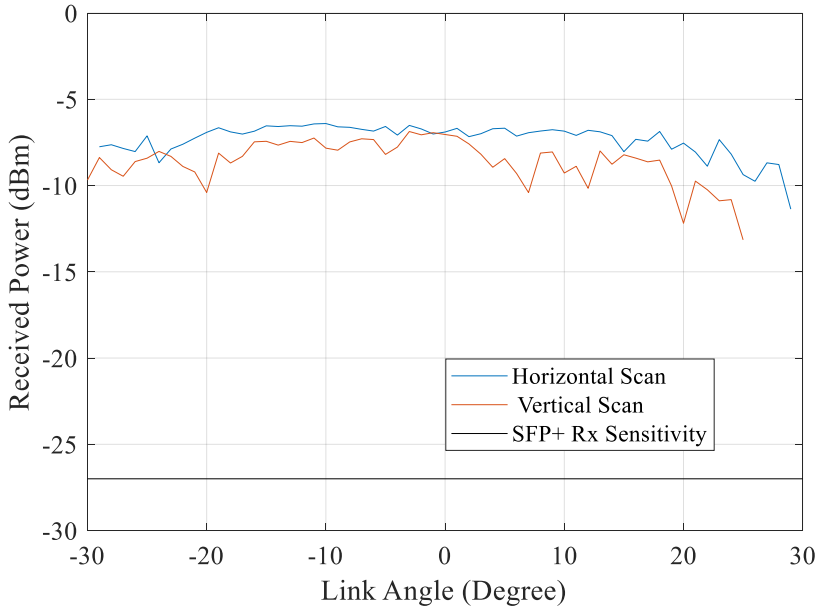


Figure 20: Received power vs transmitter rotation and steering in horizontal and vertical planes.

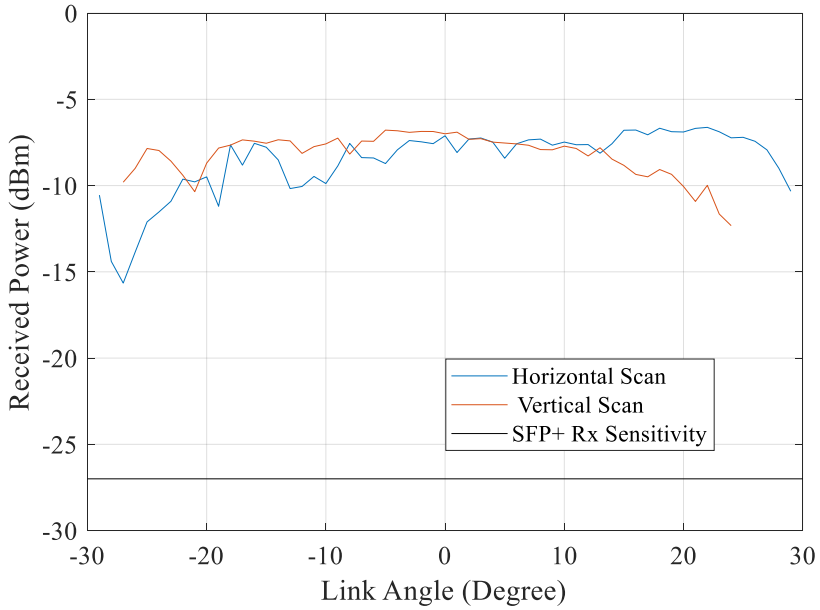


Figure 21: Received power vs receiver rotation and steering in horizontal and vertical planes.

3.2.4 Link operation and Coverage

The coverage of tracked FWF terminals was evaluated using a 10G SFP+ transceiver module (FTLX1871M3BCL) which provides 0 dBm output power at the transmitter . The receiver sensitivity was studied with a free-space 10.3 Gbit/s data transmission by placing terminals approximately bore-sight at 3.5m distance. The transmit power was reduced through the use of VOA (VOA15-APC), leading to reduction in the received power and degradation of BER. It must be noted that the SFP+ transceiver does not use any channel/line coding or channel equalisation technique. The results are shown in Figure 22. It can be seen that the receiver has a sensitivity of -27~dBm for a BER of approximately 10^{-9}. This gives a link budget of 27 dB, without any optical amplification at transmitter or receiver and also without the use of any forward error correction or channel equalisation technique.

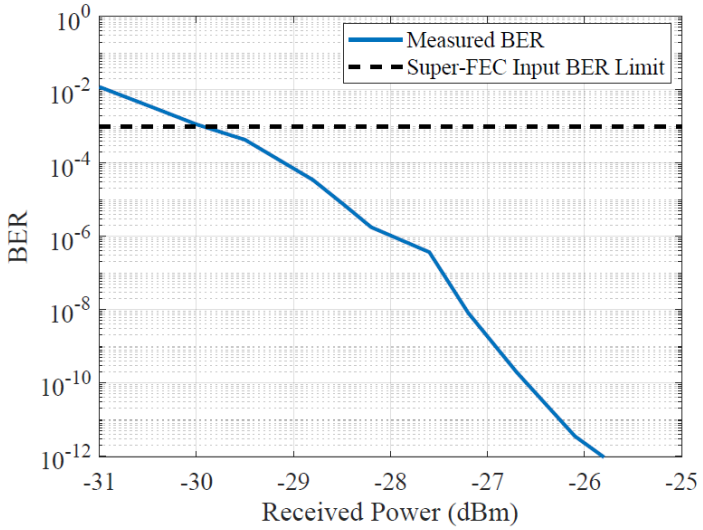


Figure 22: BER performance of FTLX1871M3BCL SFP+ module for a 10.3 Gbit/s free-space transmission.

To begin with, tracking capability of the terminals was evaluated for longest working distance on bore-sight using 10.3 Gbit/s transmission. The terminals were placed on separate trolleys at roughly 1m height and distance

between the terminals was increased and data transmission was established through tracking for different link distances. The link distance vs received power results are shown in Figure 23. It can be seen that the tracking system can provide bore-sight coverage of up to 8m with a link budget of 27dB and beyond 8m transmission can be established with a larger link budget by increasing the transmit power up to the eye-safety limit of 10dBm and by using EDFA optical amplifier at the receiver side. The link-loss increases with the link distance partly due to beam divergence and fixed accuracy of the tracking system.

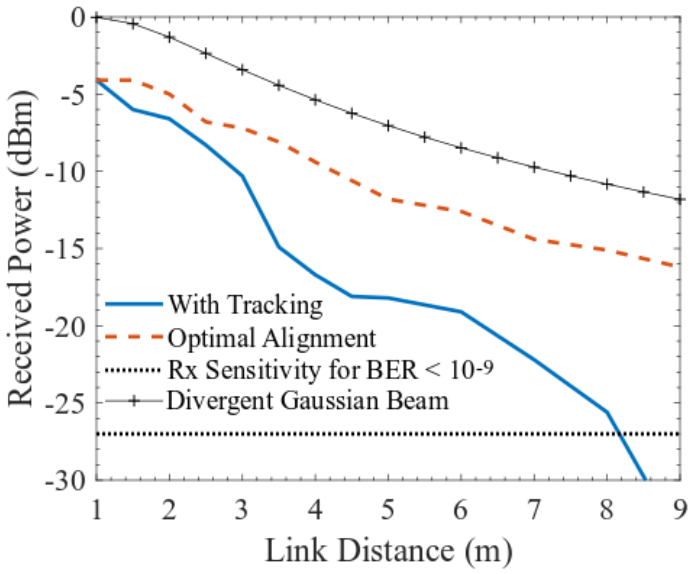


Figure 23: Bore sight communication range of FWF terminals with SFP+ based 10.3 Gbit/s free-space transmission.

Figure 23 also shows the received power vs link distance curve for optimally aligned terminals. The optimal alignment was achieved by manually 2D scanning the OptoTune mirrors within the terminals with a resolution of 0.01°. The results show that the optimal alignment can reduce the link losses by up to 10dB for a link distance of 8m and further increase link distance significantly. However, it must be noted that the manual alignment can take several hours in comparison to tracked alignment which takes < 5 seconds with MATLAB control codes.

$$P_r = P_t - L_{Gauss} - L_{Fix} - L_{Align}$$

$$L_{Gauss} = P_t \mathrm{e}^{\frac{-2R_l^2}{\omega_L^2}}$$

$$\omega_L = \omega_o \sqrt{1 + \left(\frac{L}{z_o}\right)^2}$$

$$z_o = \frac{\pi \omega_o^2}{\lambda}$$

Figure 23 also shows a theoretical curve of the received power for a divergent Gaussian beam. It is estimated by using the above equations, assuming that $L_{Fix} = 0$ and $L_{Align} = 0$, where, P_r is the received power, P_t is the transmit power, L_{Gauss} is the free space loss of a divergent Gaussian beam. L_{Align} is the link misalignment loss, R_l is the receiver radius of aperture, ω_L is the beam waist as a function of link distance L, ω_o is the 1/e beam waist at the transmitter aperture, and z_o is the Rayleigh range.

The collimator (TC06-1550) used within terminals has a full angle divergence of 0.101° and 1/e beam waist of 0.82mm. Comparing the theoretical received power with that of optimally aligned curve, it can be seen that there is 4dB additional fixed loss (L_{Fix}) in the FWF system. A small portion of this fixed loss comes from collimation and the rest comes from fiber connectors, etc. Overall the trend of the theoretical and optimally aligned received power curves is similar, while the tracked system has additional misalignment loss (L_{Align}) leading to more losses as the link distance increases.

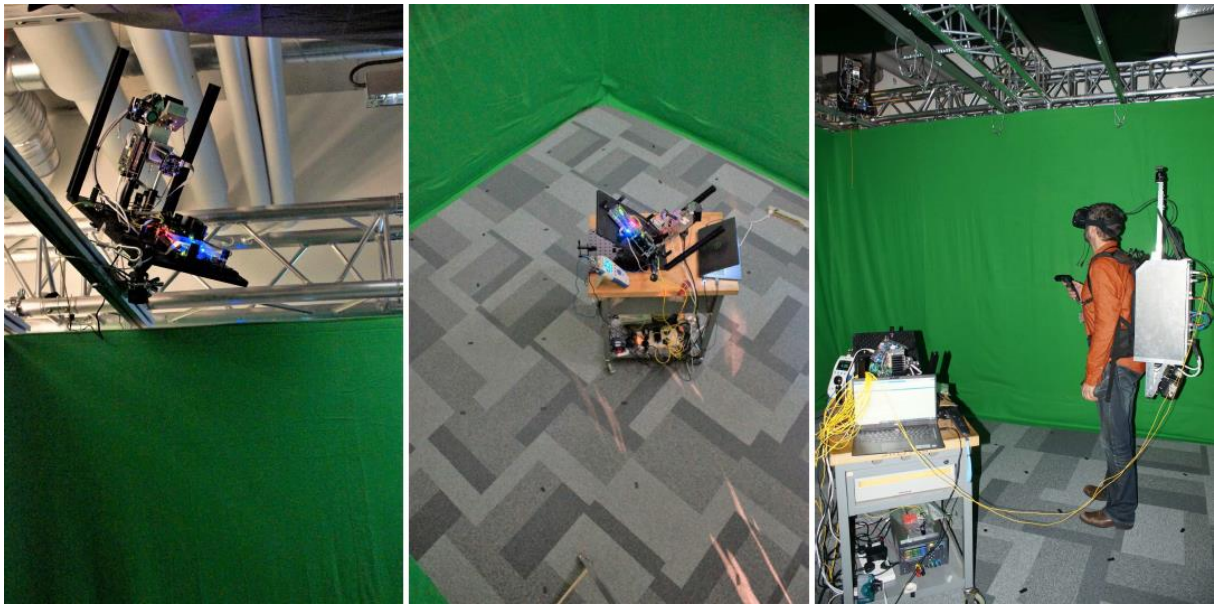


Figure 24: FWF terminal setup in 4 x 4 x 3 meter indoor testing facility at BCOM laboratory. The AP terminal in one corner at 3.5m height (left), the UE terminal on the room floor (centre) and VR-HMD connected to the UE terminal (right).

Post this, the coverage of the terminals was evaluated in a 4 x 4 x 3 meter indoor testing facility at BCOM laboratory in Rennes, France. Figure 24 shows the setup of terminals within the test facility. One terminal acted as access point (AP), mounted in one corner of the room at 3.5m height. The other terminal acted as user-equipment (UE), which was placed on a trolley so that it can be moved across the room to study achievable coverage with the 10G SFP+ transceivers.

Both up-link (UL) and down-link (DL) 10.3 Gbit/s data transmissions were performed and the terminals were aligned using the tracking system for each location of UE within the test facility. The received power was measured at each terminal when the UE moved to different locations. The results are shown in Figure 25, which reveal that the tracking system can provide approximately 4.9m^2 coverage within the 4 x 4 x 3 meter room, beyond which the tracking system is unable to work due to its limited FoV of +/- 25^o. Additionally, the 10 Gbit/s UL and DL transmissions, with limited 27dB link budget, worked well within 3.14m^2 with BER < 10^{-9}.

In addition to this, a full-duplex transmission was performed using virtual reality content. The VR-HMD was connected to the UE terminal (a video converter based onto ArriaX FPGA processing) that convert data coming from SFP+ transceiver into HDMI video. And on the other side, a VR server (based onto a GPU GTX980i) feed another video converter that convert HDMI signal into 10G eth data flow through SFP+ transceiver. This full duplex link is wholly used by the VR set up as the UL carry the video content (5.6Gbps) and the DL the localisation information (few Mbps). The video transmission was tested over different locations within the test facility and no disruption was observed. However, the use of circulators and fiber connectors for full-duplex operation induced approximately 5dB additional loss which limited the coverage to 1.5m^2 for video transmission. It is apparent that the data/video transmission coverage can be further increased to 4.9m^2 by increasing the transmit power to Class-I eye-safety limit and by using optical amplification at the receiver of each terminal.

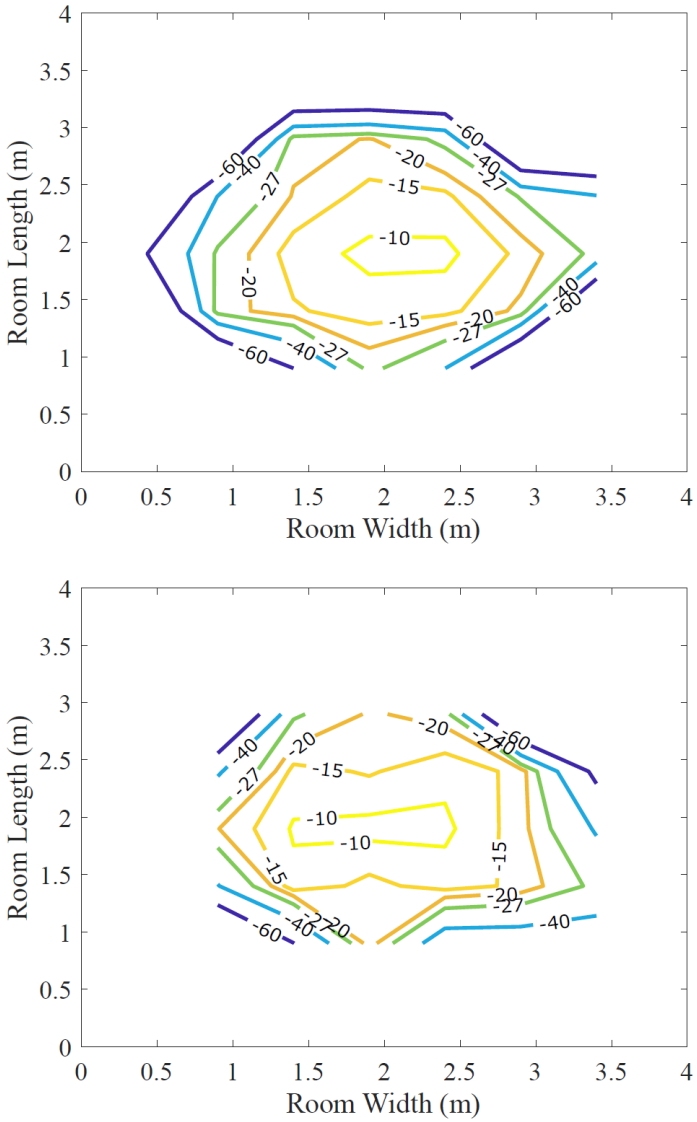


Figure 25: FWF terminal down-link (top) and up-link (bottom) received power levels (dBm) for 10.3 Gbit/s free-space transmission when the UE terminal moved across the room floor.

4 Radio link PoC

The radio data transmission system in the WORTECS project is being developed in two stages. The first stage prototype would be used in the 60 GHz band since the 240 GHz analog frontends are not available in the first and second year of the project. The final demonstrator would be working in the 240 GHz band.

The 60 GHz link developed at IHP was tested and described in D4.2 [2]. The test setup is shown in Figure 26. There are two 60 GHz modems, developed at IHP with 60 GHz analog frontends (AFEs), also developed at IHP. Anyway, commercial 60 GHz analog frontends can be also used. The modems have 1G Ethernet port that is connected to a managed 10G Ethernet switch. The switch supports 1G and 10G links. On each of the Ethernet switches test computers are connected. These computers are used to measure the performance of the link as well as to connect to the management interface of the Ethernet switches. The management interface is used to debug the connection and to monitor the throughputs of the data transferred over the wireless link. In addition, the HDMI to Ethernet converter FPGA board including a video compression/decompression functionality is connected to the 10G Ethernet switches. This system for the video is developed from B<>COM and is used to acquire the HDMI video, to compress it and to send it on the Ethernet port. This system is also used to receive the video over Ethernet, to decompress it and send it to the head mounted display (HMD). The both functionalities are at this moment implemented on a single FPGA board, in order to keep the setup as simple as possible. For the final demo, the two functionalities would be split on two separate boards.

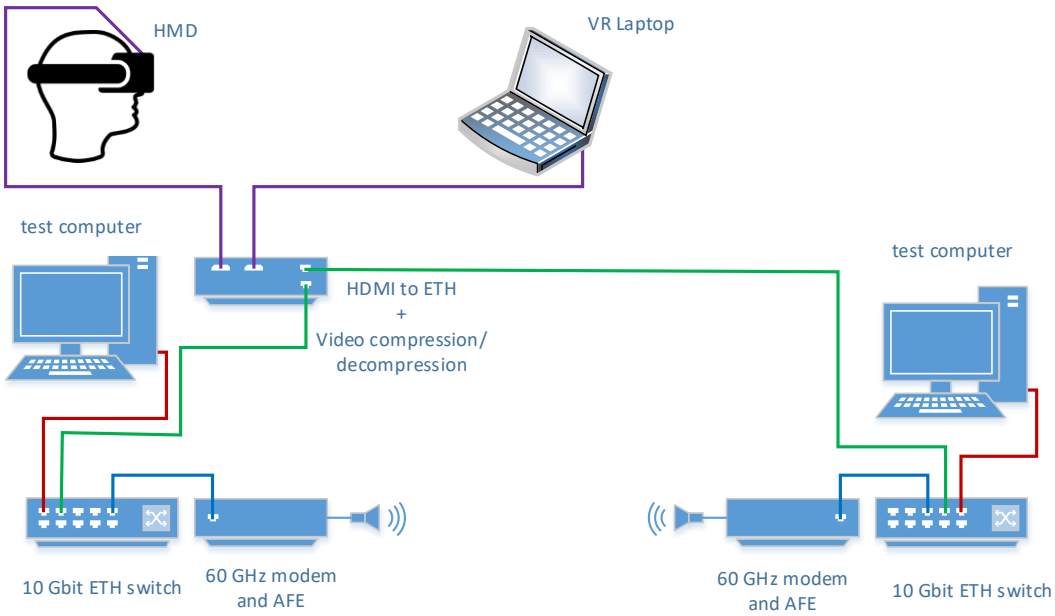


Figure 26 - Test setup for testing of the 60 GHz RF link

4.1 Features of the RF wireless link

The wireless link at this moment is capable of a 1 Gbps throughput. The baseband processor was extended and capable of 4 Gbps, but the MAC layer processor is currently being optimized to support these data rates. In addition, the digiBackBoard [3] used in this system is currently supporting 1G Ethernet and is being extended to support 10G Ethernet. A few minor problems are being encountered and currently being solved.

In order to be able to support the 1 Gbit data rate, the MAC processor should minimize the added overhead. If Ethernet frames with standard maximum transmission unit (MTU) are sent over the wireless link, a huge overhead would be introduced and the 1 Gbit throughput would be hardly reached. Therefore, the MAC layer aggregate multiple Ethernet frames in order to create a single super-frame, which can be as large as 16 kilobytes. This frame is sent to the baseband processor for transmission. When this frame is received at the other side, the MAC checks if the frame is correct and sends acknowledge. The Ethernet frames contained in the

super-frame are de-aggregated and sent to the Ethernet port of the digiBackBoard. This way, the modem establishes a seamless connection between the two Ethernet ports on the both modems.

The achievable data rate with this modem is 1 Gbps net. This data rate is achieved when optimal conditions of the link are met. The latency depends on a few factors. First the link quality affects the bit error rate (BER) and, therefore, the number of retransmissions. If the link quality is low, the number of retransmissions would be high, leading to large latency. The second issue for introducing large latency is the huge frame size of about 16 kilobytes. In order to reduce the overhead and to achieve a high data throughput, large frame sizes are necessary. The process of aggregating and de-aggregating multiple Ethernet frames introduces additional latency. Having large frames introduces also a higher probability for bit errors in a single frame, which cannot be corrected by the forward error correction (FEC). This leads to higher frame error ratio, which means also an additional average latency.

4.2 Test results

In order to evaluate the RF data transmission system, a few tests were performed, using the setup shown in Figure 26. The hardware in the loop tests and the simulation tests are described in D4.2. They would not be further discussed in this deliverable.

The two test computers have 10G Ethernet cards and are used to generate traffic in order to measure the throughput and latency. For testing the throughput, the program ***iperf3*** under CentOS was used. For testing the latency, the program ***qperf*** was used. Also, ***ping*** command was used to additionally test the latency. The HDMI to Ethernet convertor from B<>COM has also capability to measure this latency.

In Figure 2727, the test setup used and described in Figure 26 is shown.

Figure 27 - Photo of the test setup

4.2.1 Throughput measurement

In order to measure the throughput the two test computers shown in Figure 26 are used. They have 10G Ethernet ports, which are connected to the 10G Ethernet switch, and the modem (i.e. digiBackBoard) is connected to a 1G port of the Ethernet switch. The switch is managed and allows multiple options for traffic monitoring and debugging.

For throughput measurement two different software were used, *iperf3* and *qperf*. With the *iperf3* the TCP throughput was measured. In this test, the *iperf3* sends data and evaluate the performance for each one-second interval. The test lasts for 10 seconds and the throughput and the number of retransmissions are

measured. The achieved results are shown in Table 3. As can be noticed, the average TCP throughput is about 938 Mbit/s. The total number of retransmissions in the 10-second interval is 523.

Table 3 - iperf3 throughput tests

Interval [s]	Transfer [MB]	Bandwidth [Mbit/s]	Retransmissions
0.00-1.00	108	906	5
1.00-2.00	112	944	48
2.00-3.00	112	942	96
3.00-4.00	112	943	46
4.00-5.00	112	936	64
5.00-6.00	112	942	45
6.00-7.00	113	944	75
7.00-8.00	112	942	5
8.00-9.00	112	936	84
9.00-10.00	112	942	55

Additionally, the TCP and the UDP bandwidths were tested with *qperf*. The TCP throughput measured with *qperf* was 936 Mbit/s, which fits well with the *iperf3*-measured throughput of 938 Mbit/s. The UDP bandwidth measured with *qperf* is 953 Mbit/s, which is slightly higher compared to TCP, due to the smaller overhead that UDP makes.

4.2.2 Latency measurement

The latency of the radio link was also measured. A few different measurements were performed. First of all, a *ping* command was used to characterize the link latency. This test was performed by sending pings from one to the other test computer over the wireless link. The pings were sent every 0.2 seconds and a few hundred results were acquired. The mean value of the measured latency is 0.2 ms and its standard deviation is 0.053 ms. The distribution of the latency is given in Figure 28.

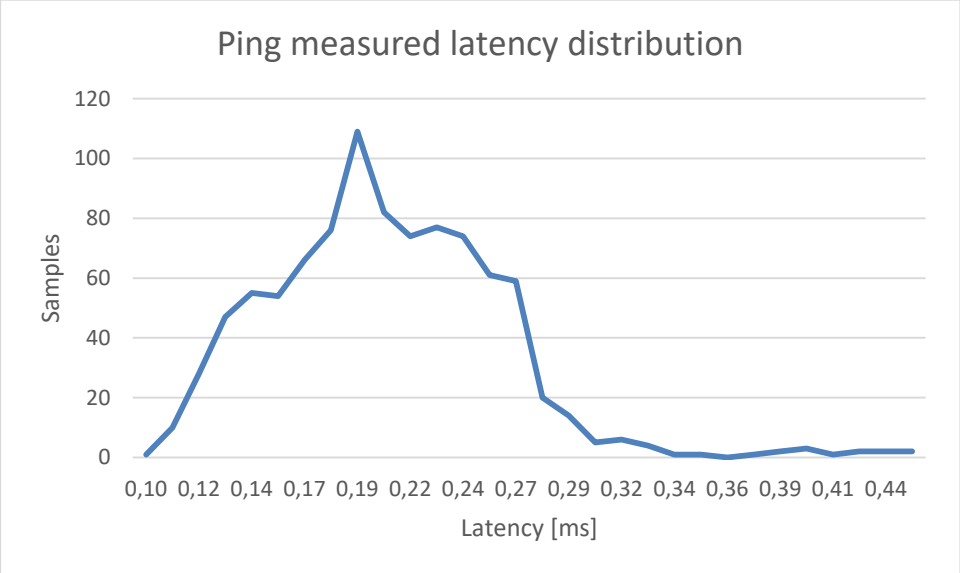


Figure 28 - Latency distribution mesured with ping command

Additionally, the latency was measured using the *qperf* command. The TCP latency was 0.138 ms and the UDP latency was 0.131 ms. Both measurements were performed when no additional data was transferred over the link, which gives the best possible latency values. It is expected that during high data rate transmissions, these values would increase slightly. These values are anyway slightly higher, since they measure the end-to-end latency including the latency of the IP stack in the test computers and the Ethernet switch latency.

The HDMI to Ethernet conversion hardware has digital outputs, which output a pulse when an Ethernet frame is send, and another output, which output a pulse when an Ethernet frame is received. Bursts of frames are sent and received for each video frame. By following the starts of these bursts, one can easily find the latency of the overall system. A scope was used to monitor these bursts of pulses and to estimate the latency of the system. In these tests a video transmission with a data rate of 860 Mbps was performed. This increased slightly the

latency of the video. The measured end-to-end latency in this case was about 0.300 ms. It was also noticeable that at some moments the measured latency goes up to 1 ms. The exact reason for this is not known at the moment but it is assumed that due to errors a frame is retransmitted which introduces an additional latency. Nevetheless, this latency is kept in the range of up to 1 ms, which fits in the budget of 3 ms which is needed in order to avoid the so called motion sickness. In Figure 29 the burst pulses for the transmitted and received frames are shown.

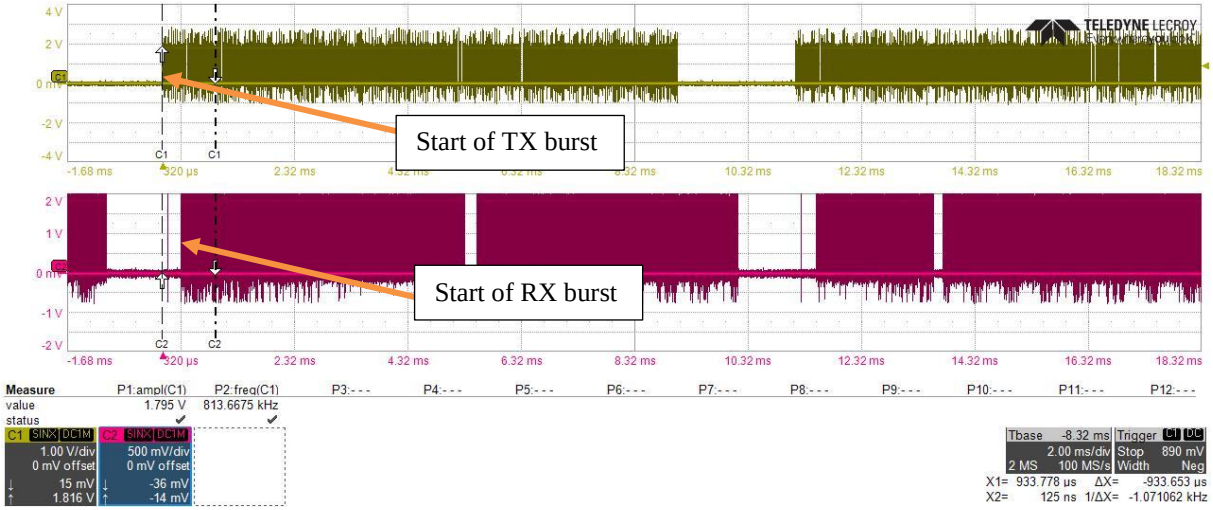


Figure 29 - Measurement of the latency using the HDMI - Ethernet converter

4.2.3 Conclusion

With the performed measurements, it was shown that video streams with data rates of less than 1 Gbps can be transmitted with low latency. The achieved latency is at maximum 1 ms and fits the needed budget for avoiding motion sickness of the user, caused by the high latency.

5 Heterogeneous Network PoC

In this section, we present the implementation of the Layer2.5 for heterogeneous networks integrated with the demonstrator V1. We mainly introduce major features of our implementation followed by the test results.

5.1 Features

In this project, we continue our work on heterogeneous networks started during the FP7 OMEGA project, based on the new communication layer located atop of the DataLink Layer (Layer 2) and below the Network Layer (Layer3), and therefore named Layer2.5.
To support ultra-high data rates, even up to Tbps, we based our implementation on an FPGA hardware platform, which enables fast packet processing. The introduction of a new communication layer demands new protocol stack at end-user devices and results in a complex implementation. Therefore, we implement this new Layer2.5 on a separate switch (on the HetNet Switch), as depicted in Figure 30, and it allows using end-user devices without any modifications.

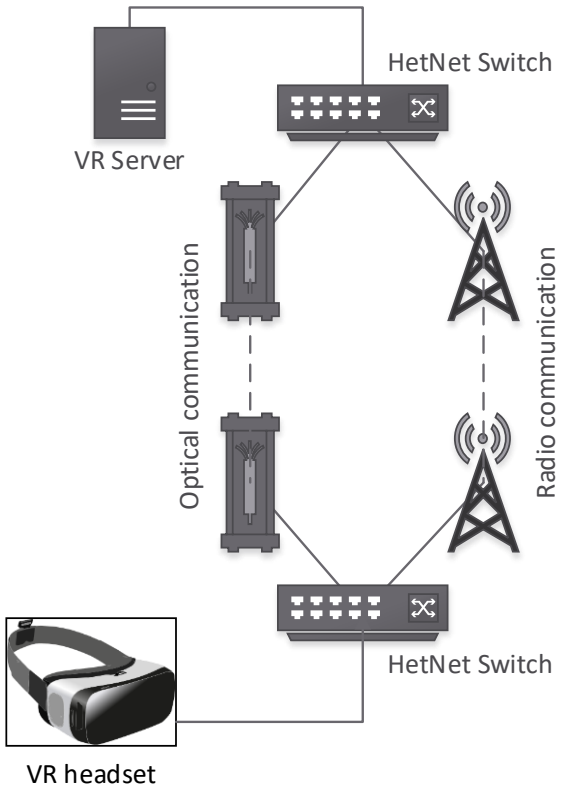


Figure 30 Heterogenous Network are support by our FPGA-based switches that implement the new Laye2.5

The main feature of the Layer2.5 is the dynamic selection of communication links for packet transmissions, based on the current link performance. In Figure 30, for instance, the HetNet switches select either optical or radio links for transmissions.
Further, dynamic link selection enables also vertical handovers, depicted in Figure 31. For instance, when the optical wireless link suffers from communication problems, the HetNet switch starts sending all packets using the radio link.
To check if links are still working, the Layer2.5 (implemented on the HetNet switches) keep sending probe frames and expect replies. If no replies arrives in a pre-defined time, the corresponding link is marked as not-working. Then, the HetNet switch sends all packets using another communication link.

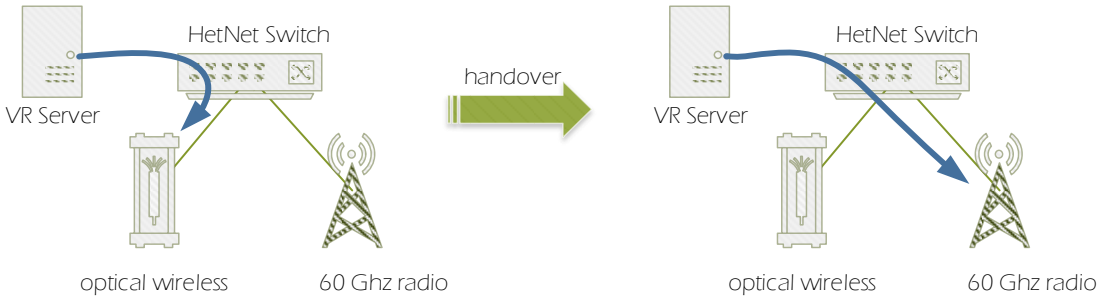


Figure 31 The HetNet switch, which implements the Layer2.5, switch the current link to another (handover), for instance, on problems with the current connection

5.2 Test results

We tested the performance of our FPGA-based data plane implementation using the iperf3 application and with the setup depicted in Figure 32. We executed the application on a standalone computer equipped with a 10 Gbps Ethernet interface. The computer generated and passed TCP traffic, using the iperf application, to the data plane running on the FPGA platform. Upon receiving frames, the data planes looked up the forwarding table and forwarded frame to another FPGA, and then to the standalone computer (to the iperf server). The iperf3 estimated the throughput, delays and packet error rates of the the TCP stream transmitted between both computers via the FPGA platform.

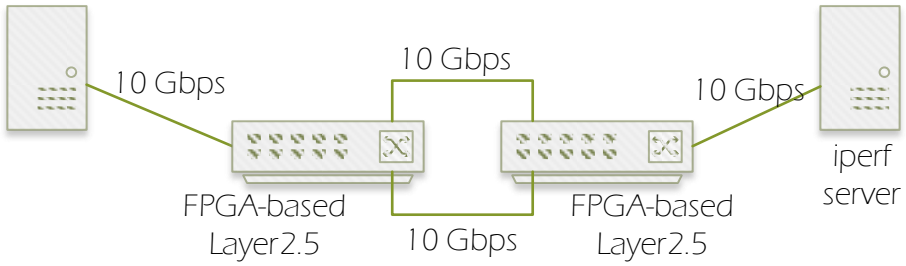


Figure 32 Test setup used to examine the throughput of the Layer2.5

5.2.1 Throughput

After adapting our design, the data plane runs stable throughout several hours tests without major problems. We measured the throughput of a single Rx/Tx lane (see Figure 32) to be 8.7 Gbps, although it should support almost 10 Gbps. We examined the problem to find the cause of a lower throughput than expected. We figure out that our data plane implementation makes about 160 ns long pauses (25 clock cycles) between sending two consecutive frames, due to our design constraints. To achieve data rates of 10 Gbps there must be no gaps between frames. It requires adapting our design by adding intermediate frame handlers and buffers, but the estimated effort goes beyond the budget available in the WORTECS project.

5.2.2 Other

We tailored our design to fit to the 10 Gbps Ethernet interface of the underlying Ethernet technology. Therefore, our major clock is derived from the Ethernet IP core: 156,25 MHz. Further, in each clock cycle each pipeline state processes 8 bytes of data and with the given clock rate we achieve a throughput of 10 Gbps (slightly less due to gaps between frames, as mentioned above).
To support higher data rates, 100 Gbps and more, we cannot really increase the clock rate. First, our design will not work with clock higher than about 200 MHz. Second, if we do not run our Layer2.5 with the same clock as the Ethernet IP core, we will run into problems of multi-clock domains. Therefore, in future design we will probably also follow the idea of using the Ethernet clock for the complete system.

Therefore, the only way to support higher data rates is to process even more data in parallel. In the simplest case, each pipeline stage must process more data, at least 80 bytes in a single clock cycle. Since our design mainly forwards all received byte without adapting them, there is almost no extra overhead in processing more bytes at once. Further, we might also add more parallel processing lanes to achieve higher data rates. However, the final solutions depend highly on the underlying Ethernet IP core. In short, we must align our design to the Ethernet IP core to avoid extra processing stages in our pipeline.

6 Video Converter PoC

In this section, we present the implementation of the video converter used during the demonstration v1. We describe some elements of the component's integration and finally we give some measure results.

6.1 Features

As a reminder, the high data throughput and the short latency imposed by the VR data setup drives to the utilization of hardware FPGA based. On the Figure 33, we present the function implemented on the two FPGAs to realize the video converters.

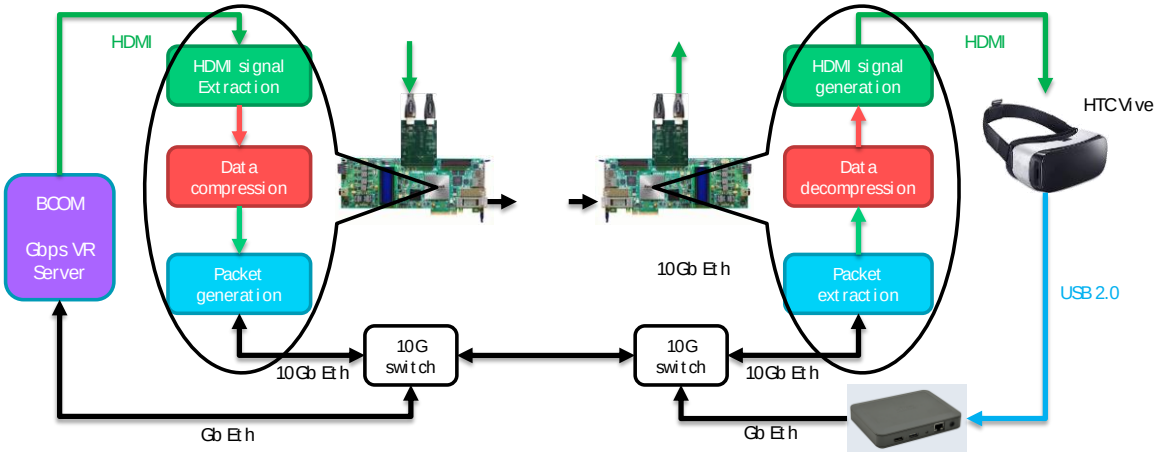


Figure 33 - Function distribution

In order to reach an easy to use prototype, we integrate all the required hardware board in a standard 2U rack. On the Figure 34, we can see the video converter rack content, with the 10G switch (top left of the picture), the DS600 USB to 1G eth converter (top right) and the FPGA board with the HDMI daughter board (on the bottom).

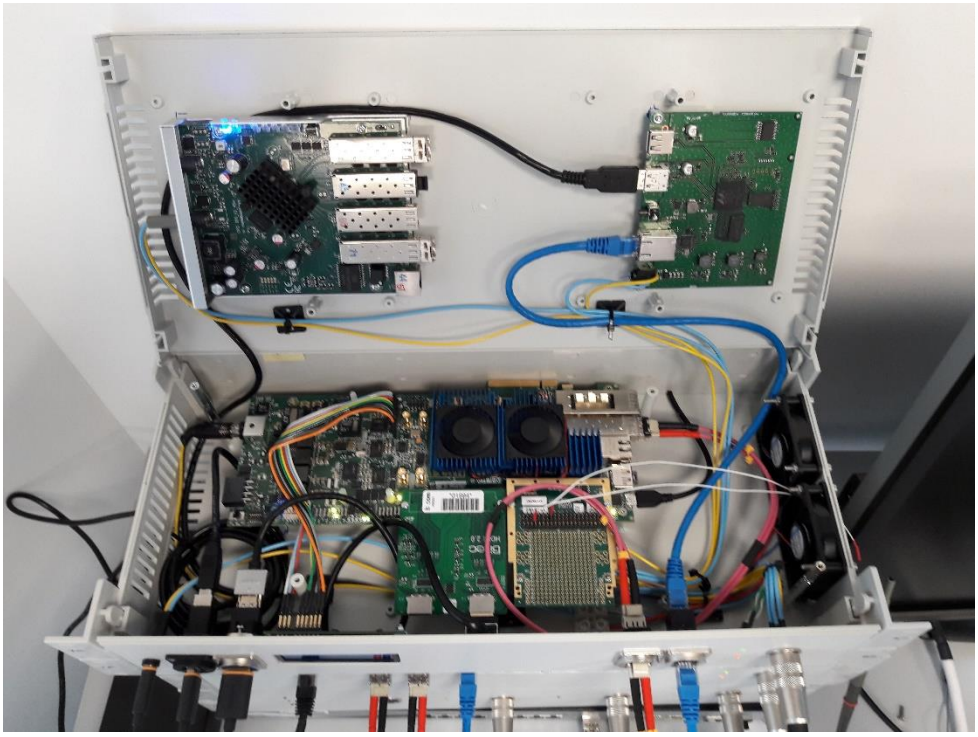


Figure 34 - Hardware integration

To realize independant test and measure, a end to end set up is used. It is composed with:

- The user HMD
- The user video converter
- The user 10G swith
- 15m of LC-LC optical fiber
- The server video converter
- The server 10G Switch
- The virtual reality server

Additionaly, as presented on the following picture, a 12V DC power supply power up all the rack, and small LC-LC optical fibers interconet the elements together.

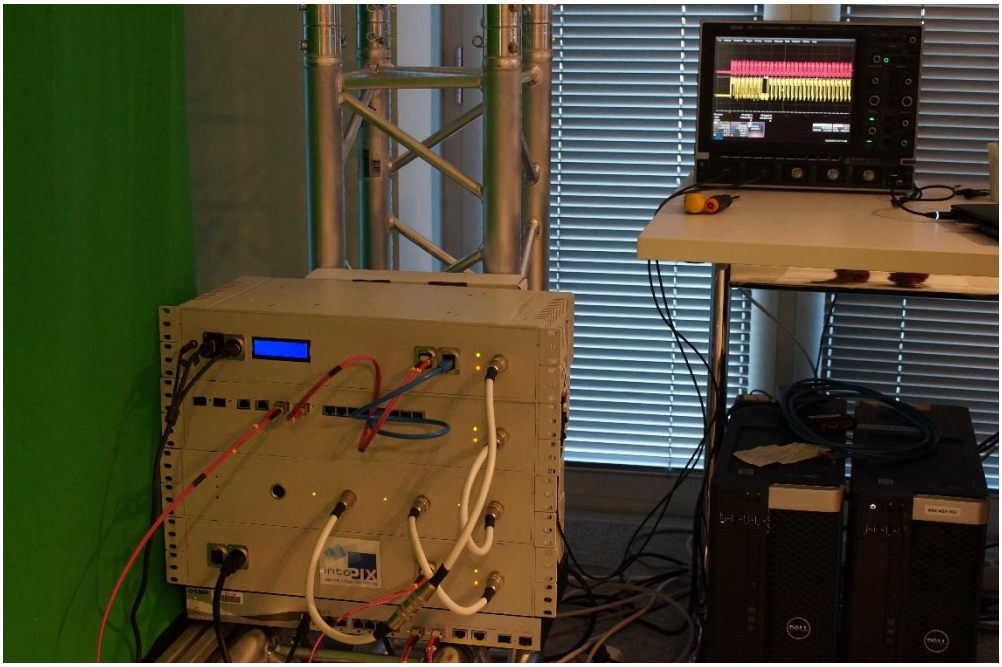


Figure 35 - User and server video converter configuration for test

6.2 Test results

Using dedicated measurement code on the FPGAs and IO connected to oscilloscope, we realized some measures of latency for the different converter's element.

6.2.1 Latency

The first measure we done is the latency of each part of the video converter. It is a critical element of the demonstrator has it should not exceed, in its totality (with HetNet and wireless link) 3ms for a full round trip delay.
On the Figure 36, we present the latency of the main components that composed the video converter. The uplink latency is mainly due to the USB to IP converter (190µs), and the main contribution of the downlink latency are the compression and un-compression IP (138+92µs), associated to the RTP des-encapsulation (250µs) module that allow some packet jitter introduced by the IP packet transmission.

The resulting round trip latency of this test set up is smaller than 700µs. That's allows some additional delay for the other elements of the total demonstrator and respect the first requirement of a maximum delay of 3ms.

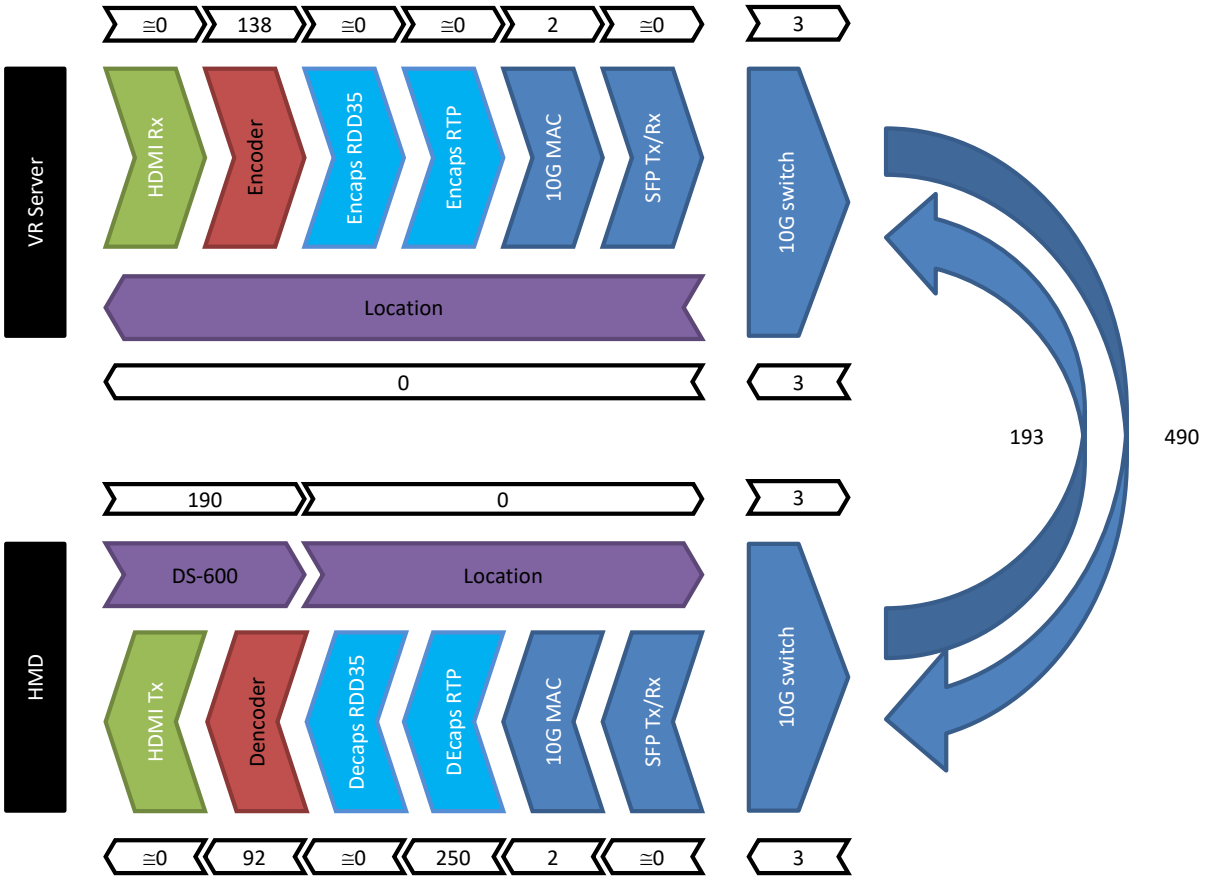


Figure 36 - Video converter modules latency

6.2.2 Compression ratio and Throughput

The video compression requires high skills in image processing and mathematical computation. A third party provider (IntoPix) provide us a compression and un-compression IP that realize this function respecting a very low processing latency.
Many compression ratio are available, but we only use two of them on this demonstrator. On the following table, the list of the available compression ratio, and in bold, the one that are used.

Table 4 – Video converter compression rate

Input bit Nb per pixel	Output bit Nb per pixel	Compression Ration	Input Throughput (Mbps)	Output Throughput (Mbps)
24	**3,5**	**6,86**	**5570**	**812**
24	4	6	5570	928
24	5	4,8	5570	1160
24	6	4	5570	1393
24	7	3,43	5570	1624
24	8	3	5570	1857
24	9	2,67	5570	2086
24	10	2,4	5570	2321
24	11	2,18	5570	2555
24	12	2	5570	2785
24	13	1,85	5570	3011
24	14	1,71	5570	3257
24	15	1,6	5570	3481
24	16	1,5	5570	3713
24	17	1,41	5570	3950
24	18	1,33	5570	4188
24	19	1,26	5570	4421
24	20	1,2	5570	4642
24	21	1,14	5570	4886
24	22	1,09	5570	5110
24	23	1,04	5570	5356
24	**24**	**1**	**5570**	**5570**

6.2.3 Packet loss or error

When using the RTP packet for the 10G Eth network, we add a packet number on each transmitted packet. This number is used to check if one packet is missing on the received data or if the packet order is good or not. Some dedicated code on the FPFA allow us to count the number of defaults that can be find in the incoming packet flow, in term of packet loss.
Additionally, we use a CRC to check the validity of the received packet. If it is not correct, the system drop the received packet because we do not have the capability to find and correct the errors it contains. This packet suppression can be either count by a dedicated bad CRC counter, or count using the packet number checker.

During long period of few hours, the system deals with VR video from the server to the HMD without any loss of packet on the user video decoder.

7 Propagation model

Propagation of light in complex environments such as indoor scenarios is typically non-tractable analytically or using numerical methods such as Finite Elements Method or Boundary Elements Method. Although the main equation to be solved is simple, the boundary conditions (effect of the scenario) turns the use of these methods very difficult. However, Monte Carlo Ray Tracing (MCRT) offers a simple but costly solution to the impulse response calculation problem in Optical Wireless Communications. Furthermore, since wavelengths below the centimetre can be treated using the ray approximation, MCRT has been proposed as a suitable solution to channel estimation also for frequencies above 60-90 GHz.

In WORTECS project, the design and implementation of a joint RF/OWC Modified MCRT simulator has been carried out, and has been detailed in previous deliverables. This document shows further advances in the channel estimation part of the project, led by ULP.

7.1 Use of Gaussians as emission patterns

MCRT is the most used algorithm family in OWC CIR estimation due to its simplicity and its flexibility. Nonetheless, these algorithms need generally long times for converging to a low-error solution. One important part that contributes to this convergence time is ray generation. The algorithm to generate random rays following a given distribution is based on the inverse method used in statistics (Equations 7.1).

$$\begin{matrix} x = F^{-1}(r) \\ r \sim U(0,1) \end{matrix} \tag{7.1}$$

Where x is the generated random variable, F is the cumulative distribution function associated to the distribution to be followed by x, and r is a uniformly distributed random variable. It must be considered that this approach relies on the existence of F's inverse. Furthermore, it is also conditioned to the existence of F itself as a primitive function. However, this does not occur much often, and numerical methods are mostly used. These methods are based on a close-value search stage followed by an interpolation (slow).

WORTECS optical emitter has been characterized as a Generalized Lambertian source, with a degeneration factor of m=20 (FWHM angle about 30º) (Equation 7.2).

$$L(\theta) = \frac{m+1}{2\,\pi}\cos^m\theta \tag{7.2}$$

The primitive function of the m-power cosine has no tractable form, since it depends on the hypergeometric infinite series. After carrying out simulations during Year 1, it was noticed that the emission pattern was very similar to a Gaussian. This led to the following mathematical analysis.

$$f_\theta(\theta) = K\,\mathfrak{F}^{-1}\{\varphi(\omega) * \varphi(\omega) * \ldots * \varphi(\omega)\} \tag{7.3}$$

Where $\mathfrak{F}^{-1}\{\cdot\}$ is the inverse Fourier transform, $\varphi(\omega)$ is the characteristic function of the pure Lambertian distribution (m=1), and K is a scaling coefficient to comply with Kolmogorov's axioms. It can be observed that the m-power cosine can be expressed as a m-fold convolution in the Fourier space. In addition, $\varphi(\omega)$ can be considered as the pdf of a dummy variable X. The m-fold convolution corresponds, therefore, to the summation of m equally distributed variables. Finally, by the Central Limit Theorem, this convolution tends to a Normal as m increases. This similarity can be analysed using Kolmogorov's distribution (Equation 7.4).

$$p = e^{-n\left(\sup|F_{1,n}(x)-F_{2,n}(x)|\right)^2} \tag{7.4}$$

Where p is the error probability of rejecting the null hypothesis, $F_1(x)$ and $F_2(x)$ are the distributions to be compared, n is the sampling size (assumed equal for both distributions), and sup is supremum. This approximation yields from Kolmogorov-Smirnov 2-sample test, and is valid for samples sizes above 100.

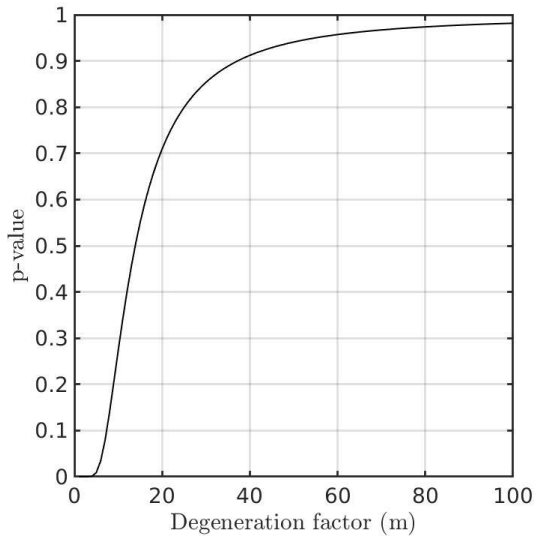


Figure 37: Error probability associated to rejecting the null hypothesis (p-value) of assuming Generalized Lambertian statistically equal to a Normal distribution.

Currently, an extensive analysis is being carried out with the objective of statistically supporting these statements analysed from the CIR viewpoint (not only at source). The obtained partial results suggest that a significant speedup can be obtained by substituting lambertians by gaussians, whilst conserving (or even outperforming) accuracy. Moreover, gaussian pseudo-random number generators are very fast compared to classical Lambertian number generators.

7.2 Standalone software development

After assessing the potential application of the developed simulation software core, its integration with a GUI was proposed. Orange provided the source files of a project in C++ as a guideline. However, the use of state-of-the-art technology is being considered. Concretely, web-based technologies such as AngularJS and ExpressJS can be embedded into desktop applications. The proposed software architecture is presented in Figure 7.2.

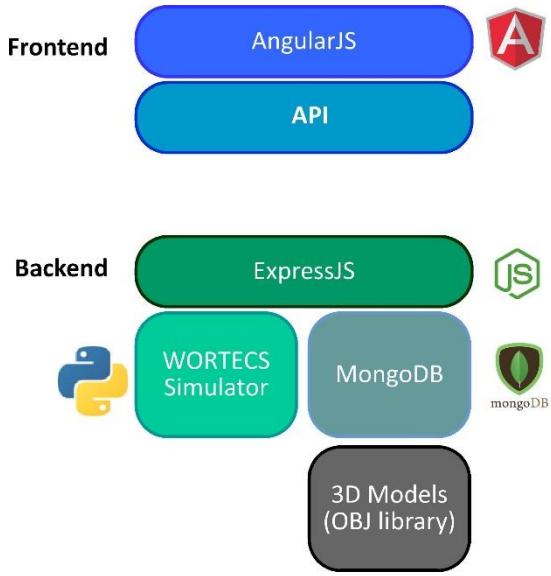


Figure 38: Proposed architecture for WORTECS' standalone CIR simulator

It can be observed that the frontend will be web-based, and the backend will comprise a database and the MCRT software, which was developed using Python. This architecture will connect front-end and Python code using a custom API.

Furthermore, this integration proposal would allow the migration of the integrated software to a cloud-based service, making the operative tasks such as updating and feature addition more reliable and easier.

7.3 Contributions to 802.11bb standard

PLF and ULP are currently collaborating in the simulation of the baseline scenarios of 802.11bb. These scenarios were simulated by Murat et al. using Zemax [4], but the results considered the combined impulse response of several perfectly-synchronized emitters. This led to a pessimistic estimation of the channel bandwidth when the receiver has more than one emitter within its field of view.

The simulation plan to better estimate the channel response will consider WORTECS' MCRT algorithm, and will take into account only one emitter, since it is a more realistic approach. The obtained results will be presented during the next 802.11bb's meetings by PLF (and ULP if possible).

8 PoC V1 overall result and conclusion

WORTECS demonstrator V1 is installed on B<>COM show room. This PoC V1 at M+24 integration and testing phase allowed us to verify, as soon as possible, the work we have to achieved offer a complete solution as defined in our objectives for the PoC V2.

We can resume the situation with the Figure 37 which could be compared to the Figure 1.

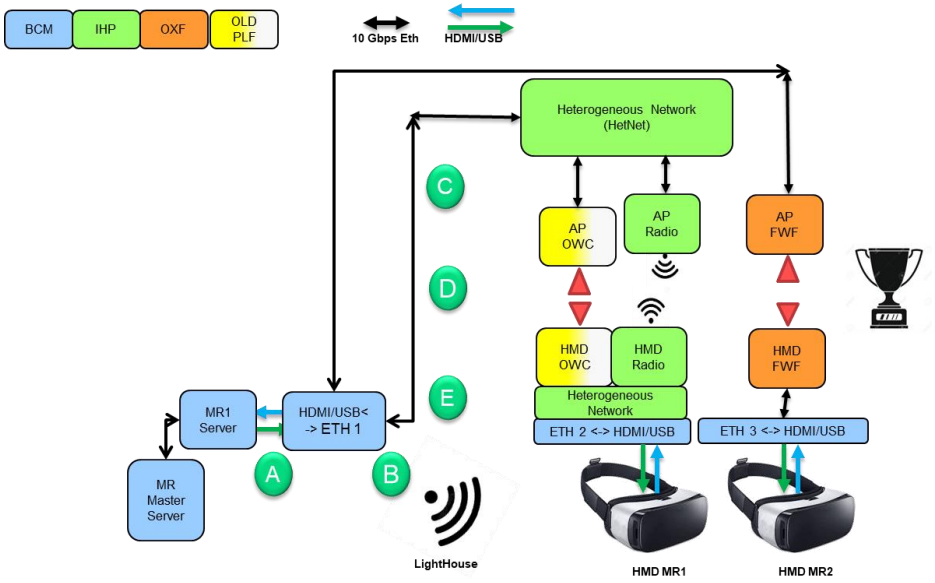


Figure 39 - WORTECS PoC V1 results

In conclusion, for the first WORTECS demonstrator version, partners have:

- Developed Optical Wireless Communication (OWC) systems design (PHY and MAC) offering (yellow and white box/OLD and PLF):
  - 650 Mbps @ 2 cm
  - 800 Mbps @ 10 cm
- Developed novel (infrared) optical steering systems with Fiber Wireless Fiber (FWF) design to deliver 10Gbps @ around $5m^2$ for point to point links (Orange box/OXF). The Terabit per second record was achieved with University of Southampton (1,16 Tbps).
- Developed radio mm-wave prototype design links operating at 60 GHz, able to deliver up to 938 Mbps with less than 0,2 ms latency (Blue and Green box/IHP and BCM).
- Developed network coordination systems (HetNet) in order to deliver up to 8,7 Gbps, with low latency, in a 2 alternative Ethernet ways (Green box/IHP).
- Developed Video Converter (VC = HDMI and USB ports to Ethernet port) prototype able to work with 10 Gbps Ethernet interface, less than 700 µs round trip latency, at ultra-high data rate (up to 5,57 Gbps) with tuneable compression ratio (from 1 to 6,86) (Blue box/BCM).
- Developed an ultra-high data rate video content “Artic Sea” for Mixed Reality V1 use case (Blue box/BCM).
- Proposed a new propagation model above 100 Ghz and up to Ultraviolet (ULP).

Problems and difficulties encountered have been well identified and efforts to succeed have been validated. The PoC Version 2 objectives remain unchanged and are in line with the initial proposal and shown in Figure 38.

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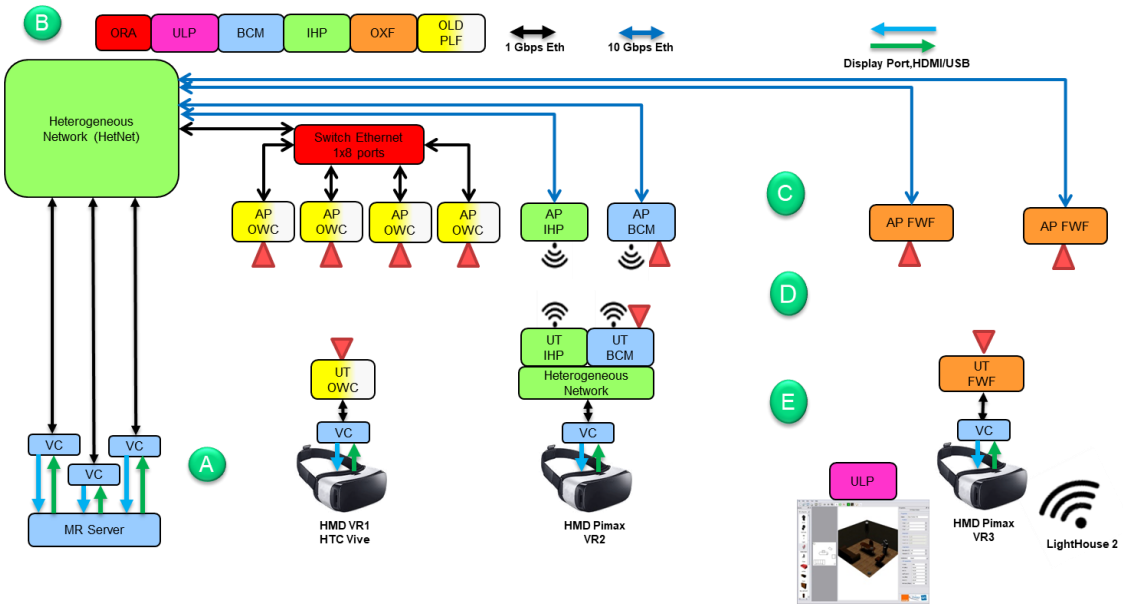

Figure 40 - WORTECS PoC V2 targets

For the period 3 and WORTECS demonstrator version 2 (7 prototypes and 1 software), partners will target:

- Video Converter – Mixte Reality server and HMD (Blue box/BCM)
  - Improve the packet loss robustness
  - Replace HTC Vive by PiMax HMD
  - DP Daughter board integration and DP IP integration
  - New low latency video compression integration (IntoPix)
- HetNet (Green box/IHP).
  - Higher throughput of HetNet switches: With extra expansions card (10 ports of 10 Gbps each)
  - Protocols study: New retransmission solutions to deal with ultra-high speed networks and limited memory
- OWC
  - PLF & OLD (yellow and white box/OLD and PLF)
    - 4APs and 2 devices, 1 Gbps
    - Follow IEEE 802.11bb progress
  - BCM (Blue box/BCM)
    - 2 wavelength, Objective 1Gbps x 2, 2m distance
- Radio
  - IHP (Green box/IHP).
    - 240 Ghz baseband and >4 Gbps real-time system
  - BCM (Blue box/BCM)
    - 60GHz patch antennas Tx/Rx
    - Wide DAC / ADC (800MHz BW on I and Q)
    - Objective 6Gbps at 4m distance
- FWF (Orange box/OXF).
  - Mobility adapted for VR applications
  - Strategy
    - Faster tracking sensor and faster software execution
    - Mount system on stabilised platform to reduce required tracking rate.
  - Roadmap
    - Design exercise on miniaturisation and industrialisation
  - Energy consumption evaluation
  - Standardization bodies investigation
- New software model design: WORTECS' MCR (Pink box/ULP).
  - Windows 10 OS
  - Integrates a generic LOS (Line Of Sight) and a modified DIF (DIFfuse) models considering rooms with furniture
  - 2D and 3D results
  - Free and simple to use.

9 References

[1] WORTECS D2.3a - Focus on Virtual Reality" Dec. 2017.

[2] WORTECS D4.2 - Radio communication prototype, October 2019

[3] M. Petri, M. Ehrig, "A SoC-based SDR Platform for Ultra-High Data Rate Broadband Communication, Radar and Localization Systems", Proc. 11th Wireless Days Conference (WD 2019), (2019)

[4] M. Uysal, F. Miramirkhani, T. Baykas, and K. Qaraqe, "IEEE 802.11bb Reference Channel Models for Indoor Environments", IEEE 802.11-18/1582r4, November 2018.