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How to achieve Terabit transmission

Synthesis of advanced research studies about PHY, MAC and Hybrid Network

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Abstract

The main objective of this deliverable is to carry out a study on wireless systems requirements needed for achieving data rates in the order of a few hundreds of gigabits up to a terabit per second (Tbps). Several technologies are envisioned: Optical Wireless Communication (OWC), Radio frequency (RF) and Fiber Wireless (FiWi). For each of them, an assessment of requirements for the PHY and MAC layer, necessary to achieve the Tbit/s objective are analysed

Keyword list

Wireless transmission ; Multi-gigabit, Terahertz, Baseband processor, radio transmission, MAC Layer, Optical Wireless Communication ; Fiber Wireless; Tbit/s; Heterogeneous Network...

Executive Summary

The THz band, covering the RF spectrum from 0.1 to 10 THz, offers channel bandwidths of 100 GHz up to 540 GHz. The optic band covers wavelengths starting from infra-red up to ultra violet. These wavelengths are considered as a main enabler for increasing data rates, going up to Tbit/s, thanks to the large spectrum bandwidth available.

Terahertz technology is revolutionary and it should support large number of applications. Additionally, the advances in the semiconductor technology enable development of new, solid state devices and their implementation in consumer products. .

The terahertz enables new B2C/B2B applications including new security solutions, mobile health, medical services (eg. cancer detection) and intra-device communications. Additionally, the THz and the optic band can be deployed in short-, mid-, and long- range applications and services including for example Internet of nano things (IoNT), long range multi-gigabit links etc.

Nevertheless, several challenges are to be addressed for the new terahertz/terabit communication technology. These challenges include:

- Identifying the most relevant B2B/B2C services requiring terabit throughputs.
- Developing an end-to-end system and network on chips that operate in the THz or Optic band, thereby enabling different range applications with throughputs up to Tbit/s.
- Implementation: The main difficulties related to the implementation and operation of Tbit/s technology is that they require a new merging heterogeneous technologies that, at the moment, are still under specification. The costs for development of these technologies require further investigation.
- The THz and the Optic band will also suffer from the similar limitations as mmWave bands in 5G: limited coverage and sensitivity to blockage. RF and/or optical localization can be implemented to ensure communication alignment into a Line-of-Sight (LoS) scenarios.

Currently, only the Fiber Wireless Fiber solution has exceeded the 1 Tbit/s target with a promising further data rate increase. This is a laboratory solution and substantial efforts must be made to reach a pre-industrial stage. The next steps would be towards improving of compactness, latency and cost.
The other technical solutions (Optical Wireless Communication and radio) and Heterogeneous Network system have the possibility of achieving this objective by using link parallelization management.
Even the THz and Optic bands are the main enabler for vast majority of 6G applications, e.g. the ones that require extremely high throughputs, it is also important that the components operating in these high frequency bands can be available at a reasonable cost and with acceptable power consumption.

Impact on the other Work-packages

This deliverable is "exercice de style" which opens the way to several possibilities for work or further studies, but mainly outside the scope of the WORTECS project.

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List of Acronyms

Acronym	Meaning
ACO-OFDM	**Asymmetrically Clipped Optical OFDM**
ADC	**Analog to Digital Converter**
A/D	**Analog to Digital**
AFE	**Analog Front End**
APD	**Avalanche Photodiode**
ASIC	**Application-Specific Integrated Circuit**
AWG	**Additive White Gaussian**
AWGN	**Additive White Gaussian Noise**
BER	**Bit Error Rate**
BP	**Believe Propagation**
CP	**Cyclic Prefix**
CIR	**Channel Impulse Response**
CFO	**Carrier Frequency Offset**
dB	**Decibel**
D/A	**Digital to Analog**
DAC	**Digital-to-Analog Converter**
DC	**Direct Current**
DCO-OFDM	**DC biased Optical OFDM**
DFT	**Discrete Fourier Transform**
DVB	**Digital Video Broadcasting**
EIRP	**Effective Isotropic Radiated Power**
FEC	**Forward Error Code**
FFC	**Free-From Optical Concentrator**
FFT	**Fast Fourier Transform**
FIR	**Finite Impulse Response**
FiWi	**Fibre Wireless Fiber**
FBMC	**Filter-Bank Multicarrier**
FOV	**Field of View**
FPGA	**Field Programmable Gate Array**
FWF	**Fiber Wireless Fiber**
FWHM	**Full Width at Half Maximum**
Gbit/s	**Giga bits per second**
GND	**Ground**
HMD	**Head Mounted Display**
HSPA	**High Speed Packet Access**
IFFT	**Inverse Fast Fourier Transform**
IM/DD	**Intensity Modulation / Direct Detection**

IR	**Infra-Red**
ISI	**Inter Symbol Interference**
LDPC	**Low Density Parity Check**
LED	**Light-Emitting Diode**
LO	**Local Oscillator**
LOS	**Line Of Sight**
LTE	**Long Term Evolution**
MAC	**Medium Access Control**
MCRT	**Monte Carlo Ray Tracing**
MCS	**Modulation and Coding Scheme**
MIMO	**Multiple-Input Multiple-Output**
NIR	**Near Infra-Red**
NLOS	**Non Line Of Sight**
OFDM	**Orthogonal Frequency Division Multiplex**
OFDM-MConst	**OFDM with multiple constellations**
OFE	**Optical Front End**
OOB	**Out Of the Band**
O-OFDM	**Optical OFDM**
ODH	**Optical Detector Head**
OTH	**Optical Transmission Head**
OWC	**Optical Wireless Communication**
PA	**Power Amplifier**
PAM- DMT	**Pulse-Amplitude-Modulated Discrete-Multitone**
PAPR	**Peak-to-Average Power Ratio**
PCB	**Printed Circuit Board**
PCC	**Parabolic Compound Concentrator**
PHy	**Physical layer**
PRBS	**Pseudo-Random Binary Sequence**
P/S	**Parallel to Serial**
QC-LDPC	**Quasi-Cyclic LDPC**
RF	**Radio Frequency**
RMS	**Root Mean Square**
SC	**Single Carrier or Successive-Cancellation**
SCL	**Successive-Cancellation List**
SISO	**Single Input Single Output**
SNR	**Signal to Noise Ratio**
S/P	**Serial to Parallel**
SP	**Sum-Product**
SPI	**Serial Peripheral Interface**
Tbit/s	**Tera bits per second**

TIR	**Total Internal Reflections**
UFMC	**Universal Filtered Multi-Carrier**
VC	**Video Converter**
VGA	**Variable Gain Amplifier**
VR	**Virtual Reality**
WORTECS	**Wireless Optical/Radio TErabit CommunicationS**
ZP	**Zero Prefix**

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1 Introduction

The main objective of this deliverable is to carry out a study on wireless systems requirements needed for achieving data rates in the order of a few hundreds of gigabits up to a terabit per second (Tbit/s). Several technologies are envisioned: Optical Wireless Communication (OWC), Radio frequency (RF) and Fiber Wireless (FiWi). For each of them, an assessment of requirements for the PHY and MAC layer, necessary to achieve the Tbit/s objective are analysed. This includes (but not limited to):

- Advanced radio and OWC system studies (PHY and MAC layers) and performance evaluation,
- High throughput and low latency coding schemes such as LDPC codes or block codes with soft decoding,
- Digital or analog (or hybrid digital/analog) MIMO/beamforming/beam steering technique either for radio or OWC,
- Integrated radio and optics front-end design,
- Modelling of impairments between antenna/LED/laser array elements,
- Novel optical concentrator, optimizing the bandwidth (BW) and the Field Of View,
- Radio and optics baseband processing methods ,
- Multi-User (MU) MIMO transmission,
- Multi-Carrier modulation such as OFDM or new prototype filters,
- Advanced radio and optical receivers using equalization technique for ISI compensation,
- Very accurate geolocation process for tracking,
- Definition of new protocols (or usage of common Ethernet),
- Compatibility with PON for backbone interface connection,
- All optical communication architecture,
- Study of fast packet forwarding between several heterogeneous wireless technologies, mainly wireless radio and optics, etc

2 Optical Wireless Communication system

We focus on a high density network that can provide >1 Gbit/s per user (full duplex) with multi user, and has a potential to provide Tbit/s per room, or coverage 'space'. This will be achieved using optical wireless communications. The OWC systems will provide bandwidth density and user data rate beyond what is available in commercial systems today, showing substantial increases up to several Gbit/s on point to multipoint scenarios.

In this section, we introduce our implementation of the physical layer (PHY) and the data link layer (DLL), which are based on the G.hn standard, for the optical wireless communication system. Firstly, the G.hn based PHY and DLL functional model are presented. Further, the digital board developed within the project is introduced. Thisboard is able to support data rates up to 1 Gbit/s for each wireless link.

2.1 PHY layer

The optical wireless communication system is implemented based on a G.hn standard PHY layer and the functional model of the PHY layer is presented in Figure 1 [1]. The physical medium-independent interface (PMI) and medium-dependent interface (MDI) are two demarcation reference points between the PHY and MAC and between PHY and the transmission medium. Internal reference points δ and α show separation between the physical medium dependent (PMD) and physical medium attachment (PMA), and between the physical coding sublayer (PCS) and PMA, respectively [1].

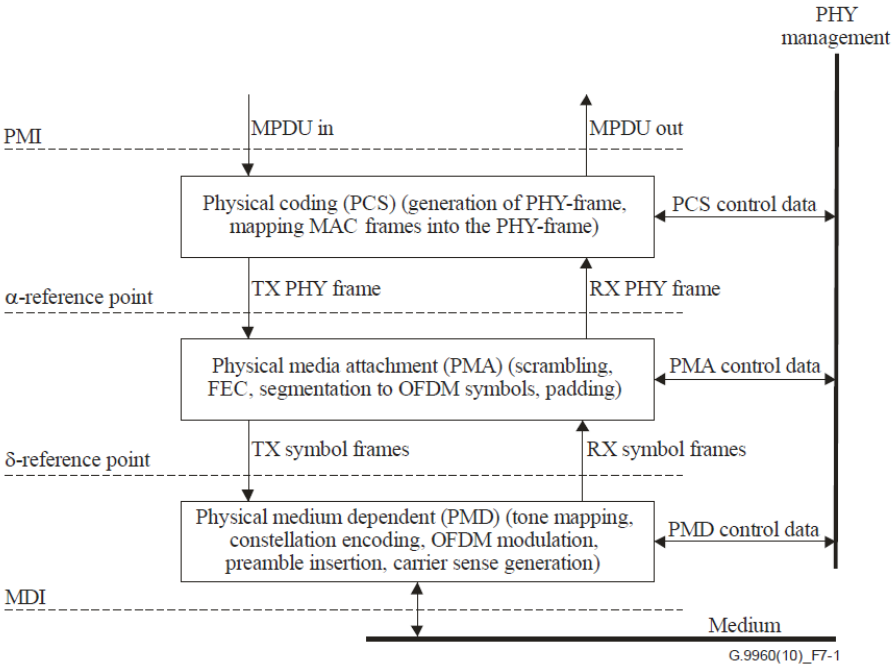

Figure 1: Funtional model of the PHY [1]

According to [1], in the transmit direction, the data input at the PHY from the MAC via the PMI in blocks of bytes named MAC protocal data units (MPDUs). The MPDU is mapped into a PHY frame in the PCS, scrambled and encoded in the PMA, modulated in the PMD and transmitted over the medium using OFDM modulation with relevant parameters. In the PMD, a preamble is added to assist synchronisation and channel estimation at the receiver. In the receiver direction, frames from the demium via the MDI are demodulated and decoded. The recovered MPDUs are forwarded to the MAC via the PMI. The recovered PHY frame headers are processed in the PHY.

The PHY is based on fast Fourier transform (FFT) OFDM modulation and low density parity-check code (LDPC) forward error correction (FEC) code. G.hn includes the capability to notch specific frequency bands to avoid interference. It also includes mechanisms to avoid interference with legacy home networking technologies. OFDM systems uses multiple orthogonal sub-carriers for the transmitted signal and each one of the sub-carrier is modulated using QAM. The maximum QAM constellation supported is 4096-QAM (12-bit QAM).

2.2 DLL layer

The functional model of the data link layer (DLL) is presented in Figure 2 [2]. The A-interface is the demarcation point between the application entity (AE) and the DLL. The PMI interface is the demarcation point between the DLL and the PHY layer. Internal reference points x1 and x2 show logical separation between the application protocol convergence (APC) and logical link control (LLC) and between the LLC and MAC, respectively.

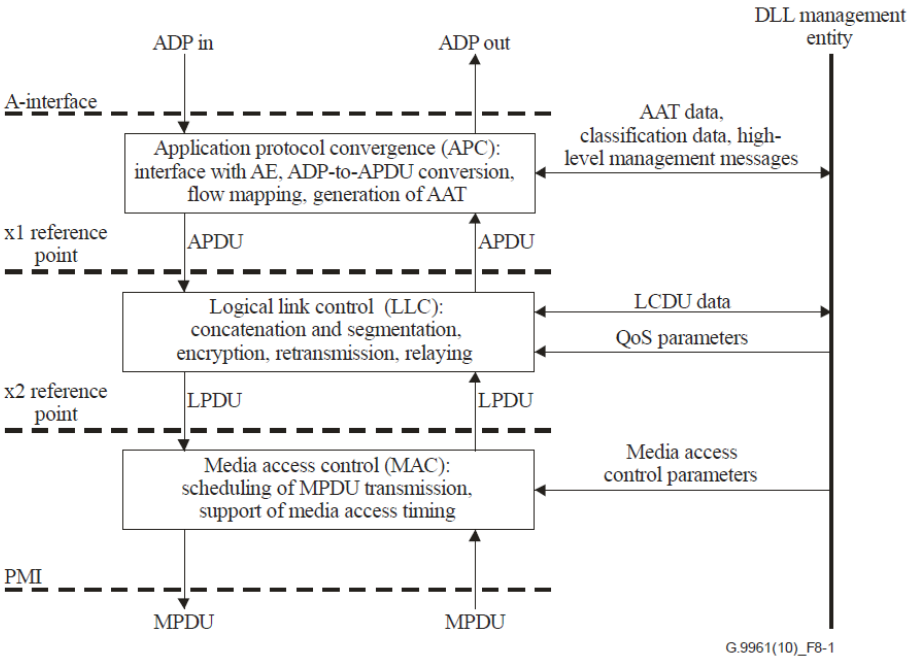

Figure 2: Functional model of the DLL [2]

The G.hn MAC is based on a time division multiple access (TDMA) architecture, in which a "domain master" schedules Transmission Opportunities (TXOPs) that can be used by one or more devices in the "domain". There are two types of TXOPs, Contention-Free Transmission Opportunities (CFTXOP) and Shared Transmission Opportunities (STXOP) [3].

Several mechanisms are used to avoid the effect of near end cross talk (NEXT) [4]:

- **MAC cycle synchronisation**: NEXT interference effect can be mitigated by synchronising transmissions between the different domains. However this is only possible if the position and if the MAC cycle start is the same in each of them.
- **Common DS/US scheduling**: The DS/US transmission need to be synchronised in order to guarantee the isolation between links.
- **Selective acknowledgements**: In order to guarantee the homogeneity of the DS/US transmissions, only delayed Acknowledgements are used.

2.3 Implementation

2.3.1 Digital Baseband Implementation

The top-level schematics of the developed digital board is shown in Figure 3.

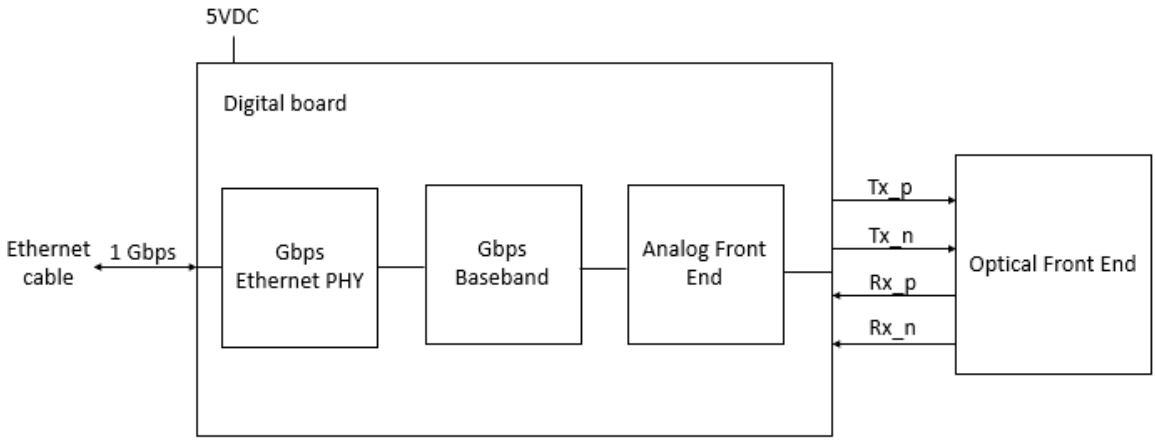

Figure 3: Digital board overview

The Ethernet interface shall be a 1000 Mbps interface. The Gbit/s baseband module features a MaxLinear wave-2 G.hn digital baseband processor [5]. The device implements the G.hn standard providing up to 2 Gbit/s . The device includes:

- A G.hn data path, which implements a G.hn PHY as specified in [1].
- Hardware functions of the G.hn DLL layers specified in [2].

The analog front end module features a MaxLinear wave-2 G.hn AFE with a single transmission and reception channel to enable SISO 200 MHz operation [6]. Transmission path comprises a programmable trans-impedance amplifier, a filter, and a line driver to condition and amplify the OFDM signal from the DAC up to a level suitable for the medium [6].

2.3.2 Optical Front End implementation

The analog front-end included in the digital baseband previously described is connected to an optical front-end which role is to convert the analog data signal to transmit into an optical signal and conversely to convert the optical data signal received into an analog signal that will be conveyed to the baseband via the analog front-end. The high-level architecture of the OFE is represented on figure here under.

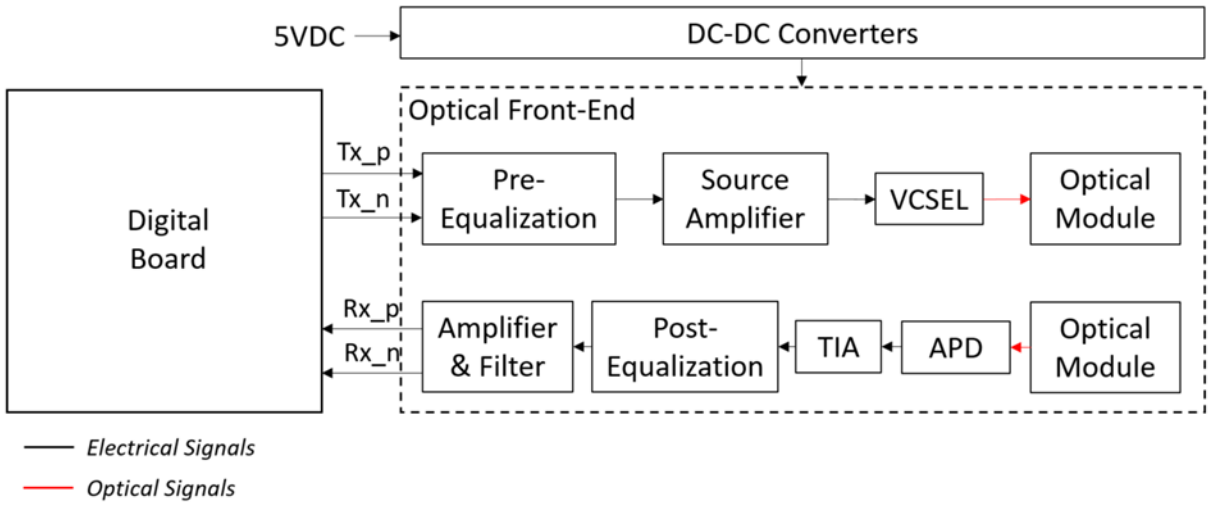

Figure 4: Optical front-end overview.

On the transmitting path, it is composed of a pre-equalization stage followed by source amplifier to format the input differential analog signal (Tx_p and Tx_n) into a DC+AC signal suited to drive the light source. This light source is here a VCSEL with 400MHz+ bandwidth, which is followed by an optical module used to reshape the non-coherent light beam pattern produced by the VCSEL.

On the receiving path, an optical model, more precisely an optical concentrator, is used to focus the incoming light beam toward an avalanche photodiode (APD) with low capacitance and high bandwidth. A trans-impedance amplifier (TIA) is then used to convert the photocurrent produced by the APD into a voltage signal that is then processed via post-equalization, filtering and amplification stages.

More details about this 1 Gb/s OWC demonstrator can be found in Deliverable 4.5 “Optical Wireless Communications Proof-of-Concept”.

2.4 Toward Tbit/s OWC Systems

The OWC system previously described enables point-to-multipoint communication with a cell capacity of 1 Gb/s for up to 16 users. In order to increase this capacity up to the Tb/s, several methods can be implemented and combined together.

First of all, the PHY data rate at a given wavelength can be increased by improving the spectral efficiency of the modulation scheme used as well as the exploitable modulation bandwidth of the light source and the photoreceiver. For example, some lasers, VCSEL and small area avalanche photodiode can provide multi GHz bandwidth that can be exploited with great benefit by multi-carrier modulations to increase the number of carriers and thus the data rate.

The number of parallel channels at different wavelength can then be multiplied using the well know wavelength division multiplexing (WDM) technique in order to further increase the capacity of the system. The quality of service can then be increased at the user level by optimizing the SNR of the signal received. This can be done by ensuring the good alignment between a focused and narrow beam transmitter and the receiver. Therefore, tracking mechanisms are necessary to monitor the mobile user position and beam-steering techniques are needed to orientate the multiple transmitted light beam toward the multiple users.

The FiWi system that is now going to be described shows how to combine these different techniques in order to reach the Tb/s.

3 Fiber Wireless Fiber

As 5G communications systems are rolled out attention is moving towards “Beyond 5G” technologies. Critical to this endeavour will be new regions of spectrum, and technologies that can use these regions and provide wireless communications. Optical wireless can access a huge region of spectrum, and this is a rapidly growing area of commercial interest, with new products and recently agreed new standards.

Looking towards Tbit/s rate optical wireless communications there are multiple challenges, concerning the modulation of light, the detection of light, and the architectures that can route data flows of this magnitude. Many of these challenges have been solved for fibre communications, where such rates can be supported with relatively mature technologies.

Using “light from the fibre” for wireless data transmission is very attractive. The light from the fibre can be collimated, forming a narrow parallel beam that can be steered from a transmitter to a receiver. A receiver based steering system can then couple the light back into a fibre, where fibre based transceivers can be used to detect incoming data streams. Work in the EC funded WORTECS [7] project, in collaboration with the University of Southampton and the UK EPSRC funded COALESCE [8] project, has demonstrated Tbit/s transmission using a fibre-wireless-fibre system [9].

Figure 5 shows a schematic of the system. This consists of two terminals, with a high-precision tracking system which allows each terminal to accurately point at the other. The transmitting terminal then sends a narrow, parallel beam of light from an optical fibre to the receiving terminal. Figure 6 shows a picture of the tracking terminals.

Once the terminals are aligned data can be sent in both directions, allowing a wireless extension of the optical fibre network. The result shows the potential to create the ultra-high rate optical wireless links that will be required for 5G and beyond and applications such as Virtual Reality Headsets.

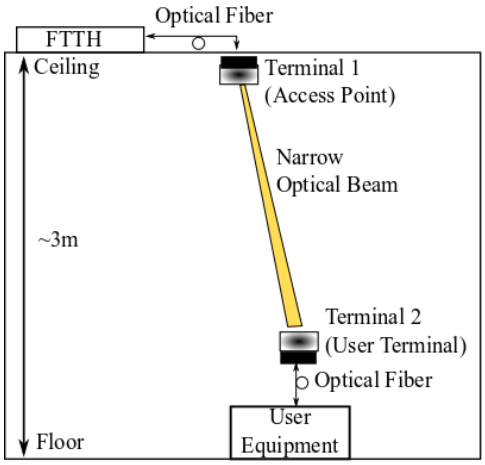

Figure 5: Terabit per second link in an indoor environment

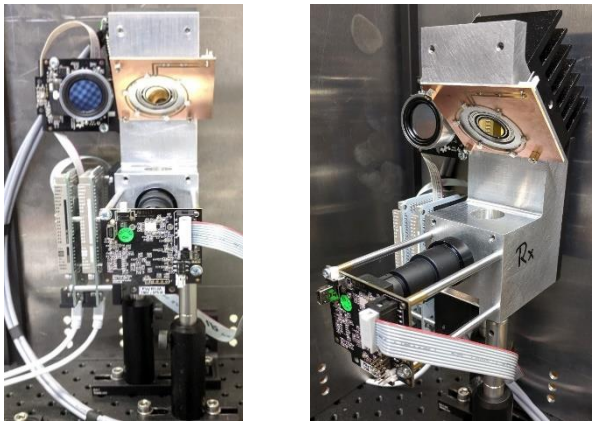

Figure 6: Transmitter (left) and Receiver (Right)

4 Radio system

4.1 PHY layer

The demand for higher data rates in RF wireless systems is constantly increasing. The available spectrum on the other hand is becoming overcrowded. This is especially true for the ISM bands where no licensing is required. The sub-6GHz ISM bands offer a couple of hundred megahertz of license free bands. These bands are mainly used for WiFi and are pretty crowded. Additionally, in order to control the interference between the devices utilizing the same wireless channel, the output power of the transmitter is strictly limited. This differs from country to country, allowing for example a bit higher transmit power in the US.

In order to increase the maximal data rate a few different approaches are being used in the sub-6 GHz WiFi systems. For example, channel bonding is used in order to increase the channel bandwidth. This enables the devices to use channels of 20, 40, 80 or 160 MHz. The use of 160 MHz channels is already supported by some devices. Using MIMO systems is another approach to increase the maximum data rate. Nevertheless, scaling of the number of the antennas is usually limited by the device size. In IEEE 802.11ax data rates of up to 9.6 Gbit/s are envisioned with the use of 160 MHz channel bandwidth and multiple antennas allowing for multiple spatial streams.

The main limitation of the sub-6 GHz systems is the limited channel bandwidth available as well as congestion of enormous number of devices using the same channel. Therefore, the 60 GHz ISM band is becoming more popular. It offers larger channel bandwidths (500 and 2000 MHz) with at least a few channels available, depending on the regulations in different countries. In this band, data rates of up to 20 Gbit/s should be possible in devices supporting the IEEE 802.11ay standard. These high data rates would be possible due to the large channel bandwidth as well as the MIMO spatial multiplexing. Nevertheless, achieving higher data rate (> 20 Gbit/s) would be challenging mainly due to the limited bandwidth available in this band.

In order to be able to use larger channel bandwidths, the main research focus for terabit communications has shifted towards the terahertz frequencies, especially being interesting the frequencies above 275 GHz. These frequencies are not regulated and no licensing is needed. Some of the bands above 275 GHz are used for astronomy and for passive sensing. Nevertheless, there are large bands which are not used and which can be used for data communications.

In this section the main advancements that would enable terabit transmission are discussed.

4.1 Semiconductor technology and analog frontend design

Even before availability of terahertz semiconductor devices, terahertz transmission and reception was possible. Travelling wave tube (TWT) is able to achieve transmission on these high frequencies. Even today, TWTs working in the THz range are available. In [10], a TWT working in the band 640-660 GHz is reported. Even the TWTs can achieve these high frequencies, they require a pretty high supply voltages and are hardly applicable in small devices.

Today's semiconductor technologies are capable to achieve several hundreds of GHz, up to THz frequencies. Although CMOS technology is preferred for any high volume production; its performances are lagging compared to other technologies like SiGe, GaAs or InP. Nevertheless, the newest Intel 22 nm FinFET technology [11] narrows the gap between CMOS and the other III-V technologies. This CMOS technology is capable of f_t/f_{max} = 300/450 GHz. This enables development of frontends in the bands below 300 GHz. Additionally, this technology enables high density integration, while at the same time being low cost. Further developments in the CMOS technology should enable use of these devices for frequencies above 300 GHz.

Currently, technologies like SiGe, GaAs and InP are capable of higher frequencies and higher output power. The main disadvantages are the higher power consumption compared to CMOS, as well as lower density integration. In Table 1 an overview of f_t and f_{max} for different technologies is given.

Table 1: f_t and f_{max} for different technologies

Semiconductor technology	f_t [GHz]	f_{max} [GHz]
IHP SiGe SG13S [15]	250	300
IHP SiGe SG13G2 [15]	300	500
IHP SiGe DOT7 [15]	505	720
Intel CMOS 22 nm FinFET [11]	300	450
InP HEMT [12]	610	1500
InP HBT [13]	521	1150
$In_{0.7}Ga_{0.3}As$ PHEMT [14]	465	1060

IHP would use the SiGe SG13G2 technology for the development of the analog frontends (AFE) working on 240 GHz. The frequencies higher than 275 GHz would not be pursued in this project since the technology used would strongly limit the performances for these frequencies. The SiGe DOT7 technology is still not mature enough and this is the reason for not using it in this project. Nevertheless, the developed circuits would be easily adoptable on frequencies higher than 300 GHz when the SiGe DOT7 technology becomes stable.

In order to achieve a higher output power, a four way power amplifier would be used at the transmitter. The topology of this amplifier is given in Figure 7. This power amplifier would give significant output power, but the efficiency would be relatively low at frequencies of 240 GHz. This means that a huge amount of energy would be converted to heat and a special precaution must be taken in order to dissipate the produced heat.

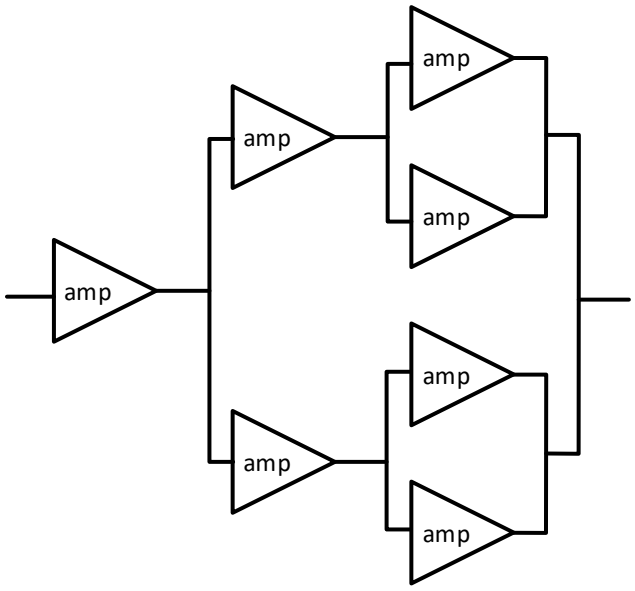

Figure 7: 4-Way amplifier

Due to the high propagation loss at these frequencies, the relatively low output power and the high noise figure of the receiver additional measures must be taken on order to enable data transmission for distances larger than a few centimetres. The first approach is to use lenses, as shown in Figure 8. The second approach is to use phased antenna array system. With this approach, each of the antenna in the phased array would have a separate power amplifier, leading to increase in the overall transmit power.

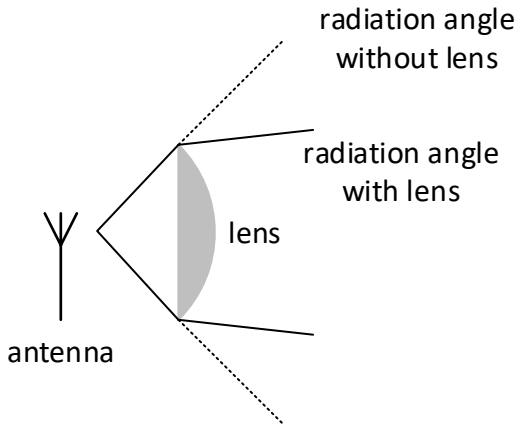

Figure 8: Using a lense to increase antenna gain

Another issue that would be addressed here is the processing of the signal with large bandwidth. The main problem which arises here is the need of high sample rate A/D and D/A converters. On the market there are just a few A/D and D/A converters which support sample rates needed to sample signals with bandwidths of more than 20 GHz. Therefore, in WORTECS is proposed to split the channel in multiple smaller sub-channels and to use A/D and D/A converters with lower sample rates. In Figure 9 a channel splitter and channel combiner are shown. They are implemented in analog domain and split/combine the channel in multiple smaller sub-channels. Another approach to address the problem of large channel bandwidth is to use simpler modulation scheme, like on-off keying (OOK). For this modulation, very simple A/D and D/A converters are needed. Nevertheless, the spectral efficiency of this modulation is very low, which would strongly limit the maximal data rate.

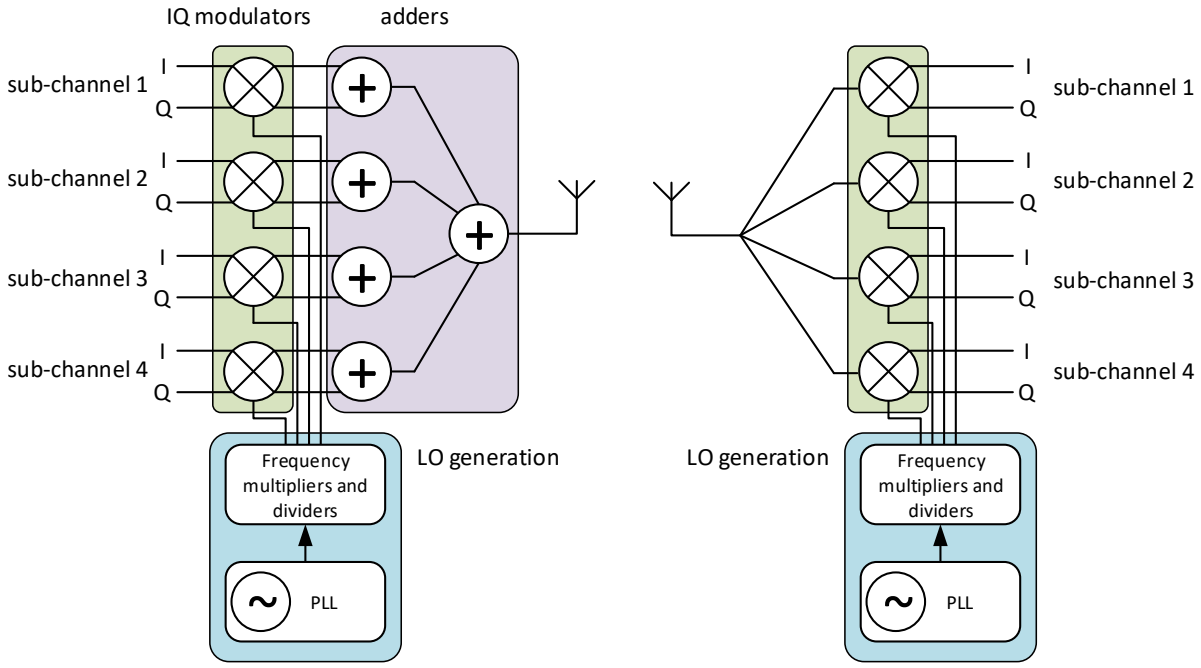

Figure 9: Channel splitter and combiner

4.2 Terahertz channel and baseband processing

The high free space path loss in the terahertz band brings special properties of the wireless channel. The transmit power of the solid state transmitters is at the moment strictly limited, usually being below 10 dBm. Additionally, the current semiconductor technologies allow only LNAs with noise figures (NF) not better than 10 dB. All these parameters forbid use of omni-directional antennas or wide radiation pattern antennas, i.e. antennas with low gain. In order to achieve significant link budget, needed for high data-rate transmission on distances of a few or

more metres, high gain antennas must be used. This would lead to narrow radiation patterns, which, on the other hand would strongly limit the multipath propagation. This means that only the direct path i.e. line-of-sight (LOS) signal would reach the receiver. Therefore, it is expected that the channel would be frequency flat. This means that there would be no need for channel equalization and if a channel equalizer is used, it can be relatively simple one.

Due to the low transmit power and the high NF of the LNA, higher order modulation schemes, like QAM64, QAM256, QAM512, would be almost impossible to be used for data transmission distances larger than a few centimetres. Therefore, the expected spectral efficiency at these frequencies would be relatively low. In order to increase the spectral efficiency, spatial multiplexing techniques like MIMO should be used. For these frequencies LOS MIMO techniques can be deployed. Additionally, different antenna polarizations for the different MIMO streams can be used.

In order to be able to process the high data rates, as mentioned before, the channel would be split in multiple sub-channels already in the analog domain. Since systems on chip (SoC) like the RFSoC family from Xilinx, include multiple giga-sample A/D and D/A converters on a single chip, this approach would be straight forward for implementation. Additionally, parallelization in the digital domain would also be needed in order to be able to process the hundreds of gigabit or even a terabit data rates. A block diagram of such a system is given in Figure 10.

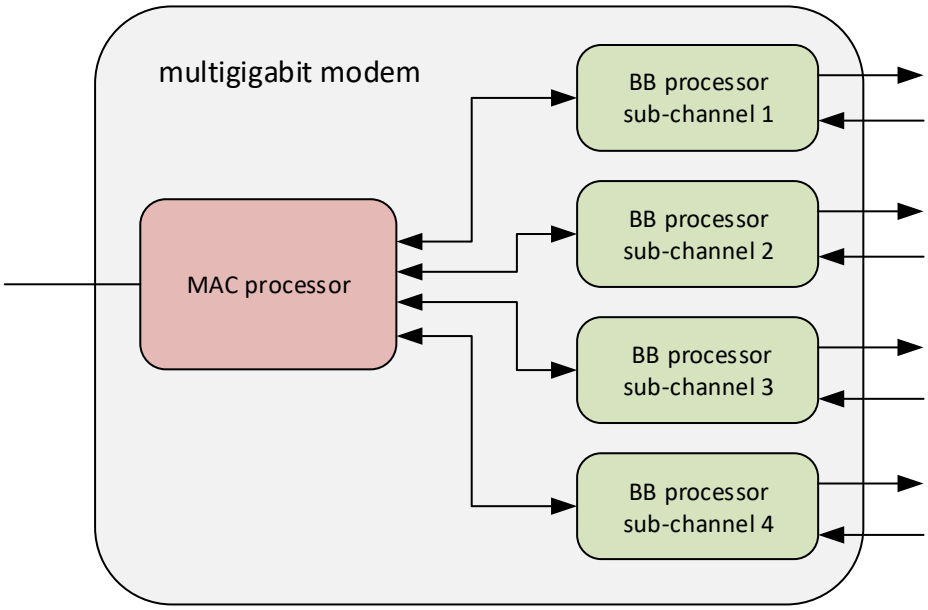

Figure 10: Multigigabit modem

4.3 MAC layer

As mentioned above, due to absence of multipath propagation, it is expected that the channel would be frequency flat. This means that the coherence bandwidth of the channel would be the channel bandwidth itself. On the other hand due to the same reason, the coherence time of the channel is also expected to be significantly large. This would allow large frames to be transmitted. This is also necessary in high data rate systems, due to the large overhead introduced by the short interframe spacing (SIFS) intervals needed before the received frames are acknowledged. Therefore, the MAC layer should be responsible for intelligent frame aggregation. This means that the MAC layer should carefully aggregate time sensitive traffic with introducing minimal latency. For non-time sensitive traffic, the latency introduced by frame aggregation is not important and larger number of frames can be aggregated.

The terahertz system in WORTECS should support point to point or point to multipoint links. The second would be used in scenarios where multiple users are connected to a single access point (AP). In the both cases, in order to support user mobility, the terahertz AFEs should have phased array antennas in order to support beam steering. The MAC layer in this case would be also responsible for beam search and beam tracking functionalities.

Since the channel would be split in multiple sub-channels, and a multiple baseband would be used, there would be also multiple data streams towards the MAC layer. The MAC layer should in this case take care about splitting the data in multiple streams and combining the multiple streams in a single data stream.

5 Heterogeneous Network system

5.1 Definition

The latest developments wireless communication can support data rates of Tbit/s (see paragraph Fiber Wireless Fiber). Alternative solution to provide high data rates with wireless communication is bonding several technologies. Further, there are also other benefits of bonding heterogeneous technologies apart from high data rates, such as higher reliability or lower latency.
More than a decade ago we were aware of benefits provided by bonded heterogeneous networks and started the EU FP7 OMEGA project [16]. In that project we combined several network technologies for home applications and supported data rates up to 1 Gbit/s. In this project we continue the work of OMEGA project and investigated bonded heterogeneous networks with much higher data rates. We mainly examined if state-of-the-art hardware can bond wireless technologies to support data rates up to 1 Tbit/s.
In this section, we introduce our experimental results of FPGA implementation and present also the feasibility study on high-speed wireless heterogeneous networks.

5.2 Implementation overview

We already introduced our implementation of heterogeneous networks in the Deliverable D3.2 and here we just give a brief overview.

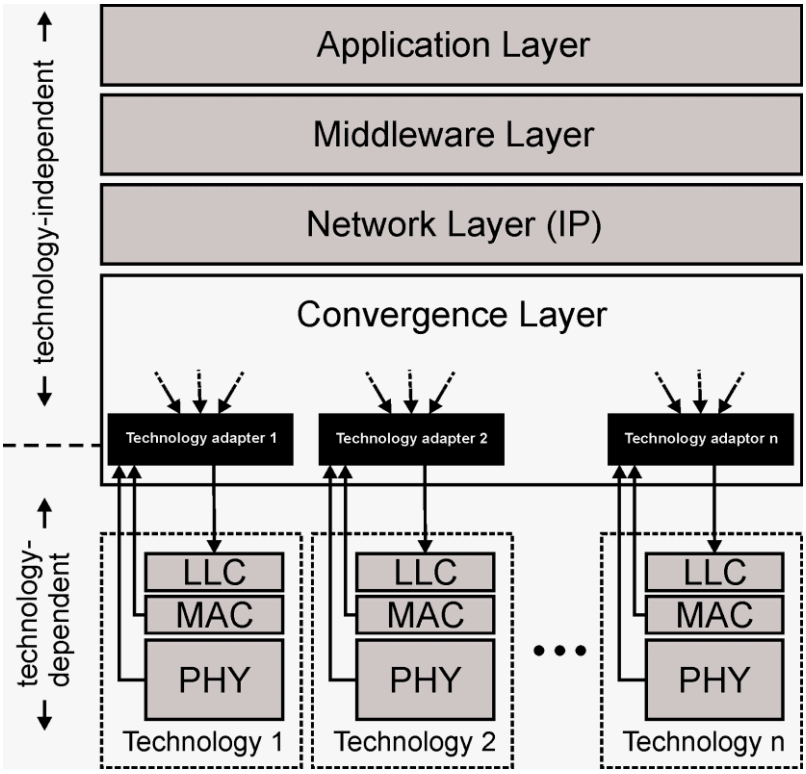

Figure 11: The InterMAC layer (Convergence Layer) integrates heterogeneous communication technologies into a single network

Based on our experience in the EU FP7 OMEGA project we integrated heterogeneous communication technologies by introducing a new communication sub-layer. We locate it atop of the Layer2 in the OSI network model and named it InterMAC (see Figure 11). However, in WORTECS project we called this new sub-layer the Layer2.5.

To benefit from the new Layer2.5 and integrated heterogeneous networks, all network devices (include end-user devices) must adapt their network protocols stack and include this new sub-layer. Clearly, it is rather infeasible, if not impossible, to adapt so many network devices. Therefore, we implemented this new layer only on network switches and enable end-user devices to benefit from Layer2.5 without adapting their protocol stack (see Figure 12).

In the OMEGA project we implemented the InterMAC in software and running as a Linux kernel module in supported data rates of 1 Gbit/s [17]. We expected that even by optimizing our software implementation we will not be able to support Tbit/s wireless networks. Therefore in WORTECS we decided to examine hardware implementation of Layer2.5 based on FPGA.

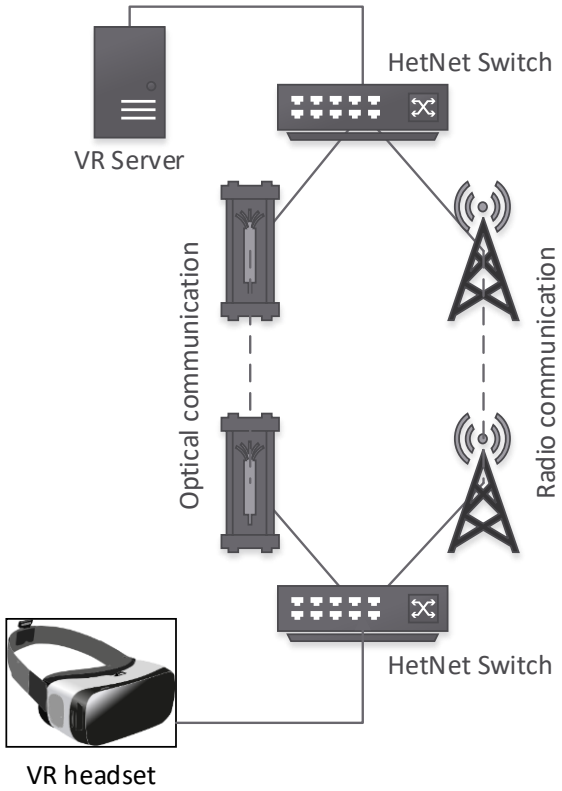

Figure 12: Implementation Layer2.5 on HetNet Switches and allow end-user devices (VR Server and VR headset) to benefit from heterogeneous networking without adapting their protocol stacks

We based our implementation and analysis on FPGA boards of Xilinx (model VC709) with four 10 Gbit/s Ethernet interfaces. Clearly, we cannot support Tbit/s network with such hardware but it still allows us to examine the Layer2.5 implementation and examine potential bottlenecks.

To enable high-sped forwarding we created a separate processing lane for each 10G Ethernet interface, as depicted in Figure 13. In this way, the FPGA processes incoming data from all physical interfaces in parallel and increase the total data throughput. In general, our Layer2.5 implemented on the FPGA resembles a network switch. It receives frames and based on the internal forwarding table, the FPGA passes frames to outgoing ports. However, any other network device can update the forwarding table by sending specific control frames. Further, the FPGA maintains also link statistics and learn about link performance used for forwarding decisions, for example, to carry out handovers in case of connection problems. More details about the implementation are already explained in the previous deliverable D3.3.

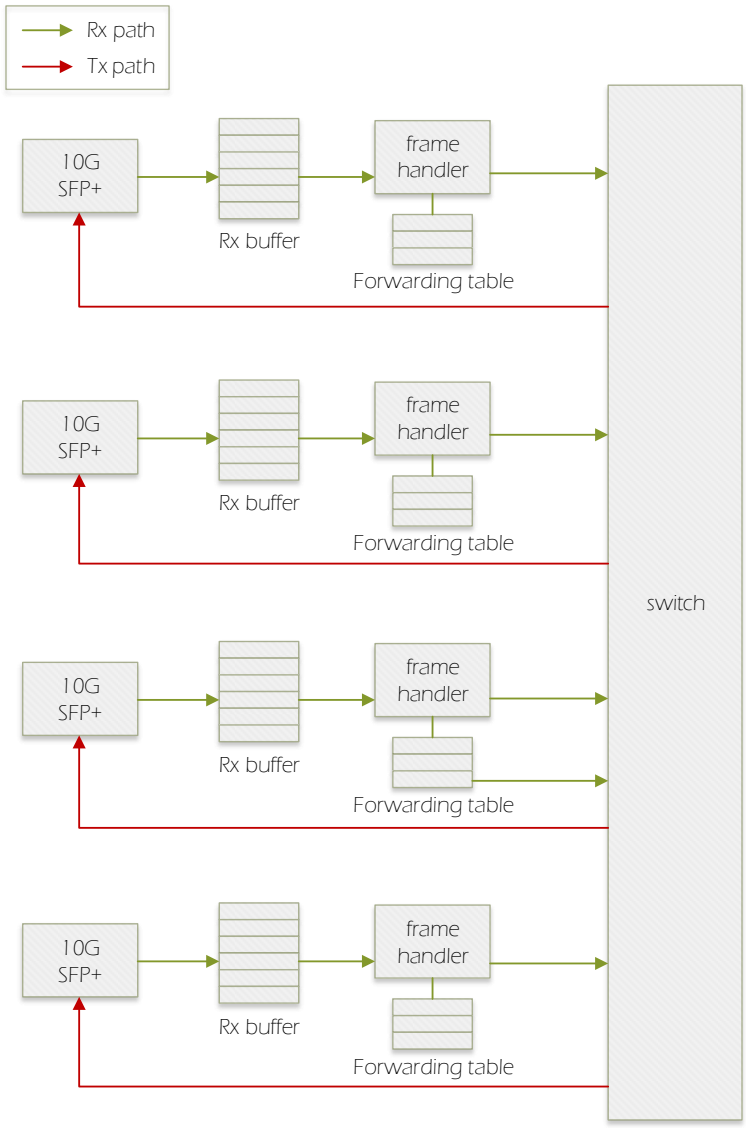

Figure 13: Data plane implementation on the VC709 FPGA platform. There are four 10 Gbit/s SFP/SFP+ interface available and therefore we created a separate lane for frame processing for each interface.

5.3 Feasibility study on Tbit/s heterogeneous networks

Although our hardware platform limited the total throughput to 40 Gbit/s, as our FPGA included four 10 Gbit/s Ethernet ports, we examined the feasibility of current and future architectures for 1 Tbit/s heterogeneous networks.

First, we examined the throughput of a single 10 Gbit/s lane for frame processing (see the architecture in Figure 13). This processing includes the following actions:

1. The Ethernet module receives the frame in 64-bit chunks (8 bytes).
2. Since the frame in the Xilinx Ethernet Module does not necessarily start at the beginning of each 64-bit data chunk, the leading bytes in front of data are removed.
3. The CRC of the Ethernet frames is removed, as frame may be adapted by other modules and the CRC must be calculated again.
4. Any extra frame headers, such as VLAN, are removed.
5. The forwarding module reads the headers from the frame and finds the outgoing port for this frame based on:
    a. The frame headers and entries in the forwarding table
    b. The current link performance of outgoing Ethernet interfaces

6. The forwarding module passes the frame with the outgoing port number to the switch module.
7. The switch passes data to the outgoing port.
8. VLAN header is added if needed, and the CRC is newly calculated
9. The Ethernet module transmits the frame.

Our Layer2.5 must carry out all these tasks very quickly, preferably in parallel, to support high data rates. We measured the throughput of a single 10 Gbit/s lane: 8.7 Gbit/s. We examined the cause of not reaching 10 Gbit/s and the problems were pauses between frames. That is, when our Layer2.5 transmits two consecutive frames, there is a gap of 25 clock cycles (about 160 ns) between these frames. Clearly, to provide 10 Gbit/s throughputs there must be no gaps between frames.

To tackle these problems, we would have to add more buffers to our design and adapt frame handlers but it goes beyond the scope of our work in this project. Nevertheless, with some more effort the design can support the total throughput available for this lane, 10 Gbit/s in this case and 40 Gbit/s when using all four lanes available.

Clearly, with this implementation we cannot achieve 1 Tbit/s packet forwarding but we use these results to estimate if state-of-the-art hardware can support such high-speed packet processing of Layer2.5.

Although we already use four lanes in our implementation to allow parallel packet processing and increase the total throughput, we still need more such processing lanes for high-speed networks. However, the number of processing lanes is limited by available space on the FPGA. Therefore, we estimated the total space occupied by our implementation based on four parallel lanes and it needs about 16% of the total FPGA space. Based on our experience, we can use about 80% of all resources available, otherwise the synthesis tool (Vivado of Xilinx) runs into problems with placing and routing. Therefore, we could add 5 more lanes than we have now and in theory we could increase the throughput by factor 5. As now we support almost 40 Gbit/s (10 Gbit/s on each single lane, provided we will adapt our implementation to fix the 8.7 Gbit/s limit on each lane), this FPGA could support even 200 Gbit/s. However, due to some constraints, such as extra processing needed to split and merge data from several lanes, the total throughput would be smaller than 200 Gbit/s.

We tailored our design to fit to the 10 Gbit/s Ethernet interface of the underlying Ethernet technology. Therefore, our major clock is derived from the Ethernet IP core: 156,25 MHz. Further, in each clock cycle each pipeline state (e.g. frame handler or switch in Figure 10) processes 8 bytes of data and with the given clock rate we achieve a throughput of 10 Gbit/s (slightly less due to gaps between frames, as mentioned above). To support higher data rates we cannot simply increase the clock rate. First, our design will not work with clock higher than about 200 MHz. Second, if we do not run our Layer2.5 with the same clock as the Ethernet IP core, we will run into problems of multi-clock domains. Therefore, in future design we will probably also follow the idea of using the Ethernet clock for the complete system.

The major approach to increase the data rate in again is using more parallel processing. Previously, we examined using more parallel lanes for packet processing. Here, we consider reading, processing, and transmitting more data bits in a single clock cycle. For future Tbit/s networks we will rather use faster physical interfaces, for example, 100 Gbit/s Ethernet. In this case, the Xilinx Ethernet IP core provides 64 bytes in a single clock cycle, that is, 8 times more than our current 10G interfaces. Therefore, by only using faster physical interfaces and processing more data bits in a clock cycle, we would increase the total FPGA throughput 8 times. Since our design mainly forwards all received byte without adapting them, there is almost no extra overhead in processing more bytes at once. Further, it will also not lead to significant changes in the number of resources occupied on the FPGA. Therefore, we could even achieve 8 times higher throughput by processing 8 times more data bits in a clock cycle.

Based on our current design we examined potential throughput of our design tailored for future FPGA boards with 100 Gbit/s Ethernet interfaces. First, we can add at least 5 times more parallel packet processing lanes on current FPGA, and future FPGA boards will probably provide even more resources and allow more processing lanes. Second, faster physical network interfaces allow processing of more data in a single clock cycle. For example, the Xilinx 100 Gbit/s interface provides 8 times more data than the currently used 10 Gbit/s interfaces. All in all, by using only these two means we can theoretically increase the total throughput by 40 times, that is, up to 1.6 Tbit/s. The final throughput will probably be smaller due to some hardware restrictions and the need of extra processing for splitting of merging several parallel lanes. However, the final throughput, based on more powerful hardware, will be much higher than our current implementation and probably it will reach 1 Tbit/s data rate.

5.4 Integration with high-speed switches

We expect that future networks will have to bond various communication links and therefore we examined their efficient integration. From the technical point of view, our Layer2.5 needs several physical interfaces to bond various networking technologies. We based our implementation on the VC709 FPGA board, which provide only four 10G Ethernet ports by default. One of these ports is connection to the Virtual Reality server, as depicted in Figure 14, and three remaining ports are available for connecting various communication links. Clearly, the number of supported heterogeneous networking technologies is limited by the number of physical ports available on our FPGA.

Similar problems will probably arise also in future real network applications. Obviously, the simplest way to deal with this problem is to enable more ports on the HetNet switch (HS). However, for some applications it is not always feasible from several reasons. More hardware ports mean also more complex design, resulting in extra cost. Further, we need also more processing for more ports, and it occupies more FPGA resources. For such applications we examined a flexible way of increasing the number of physical ports to support more heterogeneous network technologies.

Figure 14 depicts the idea using extra physical connections based on the network switch (NS) connected to the FPGA, to the HetNet switch. In this case, three network technologies: two access points of optical wireless communication and the 240 GHz radio link, are connected to the network switch. However, without extra changes this setup will not work well. When the HS sends the frame to the NS, it must select the transmission technology connected to the specific outgoing port of the NS. However, in the default setup there is no way the FPGA selects the outgoing port of the network switch.

However, we can adapt the architecture presented in Figure 14 to for the needs of Layer2.5 by using virtual LANs (VLAN). Although the VLAN were introduced mainly to separate several networks within a large organization, we use them in this case to allow the HetNet switch to determine the outgoing port of the network switch. Therefore, we defined the link between the HetNet and network switch as so called Trunk Link, and we treat each heterogeneous network connection as a separate virtual LAN.

In short, on receiving data from the VR server, the HetNet switch looks for outgoing communication link. If the link is directly connected to the FPGA (for example, Future Radio Technology in Figure 14), it just passes the frame to the outgoing port. However, if the outgoing port is connected to the network switch, the FPGA must inform the switch which outgoing port to use. Therefore, the HetNet switch adds the VLAN header (see Figure 15), which includes the virtual network number. In this application, each technology connected to the NS has a specific VLAN number assigned to it and both switches (HS and NS) know these numbers. On receiving the frame from the HS, the network switch reads the VLAN header and learns about the outgoing port for this frame. Then, it removes the VLAN header and passes the frame to the corresponding port.

It works similarly on the way back to the VR server and the HetNet switch receives frames with the VLAN header form the NS. Based on the VLAN header the HS knows the heterogeneous technology used for transmission.

To verify the idea of using VLAN for the integration of Layer3.5 and network switch we implemented the major VLAN functionality on FPGA and configured the network switch appropriately. That is, the Layer2.5 supports adding and removing of VLAN headers. With our implementation we verified that by with VLAN our Layr2.5 works well with 10G network switch and in this way we can add more physical interfaces to our HetNet setup

Obviously, the new physical interfaces of the network switch don’t increase the total throughput of the HetNet switch. We use them only to allow more heterogeneous technologies to be used with our architecture.

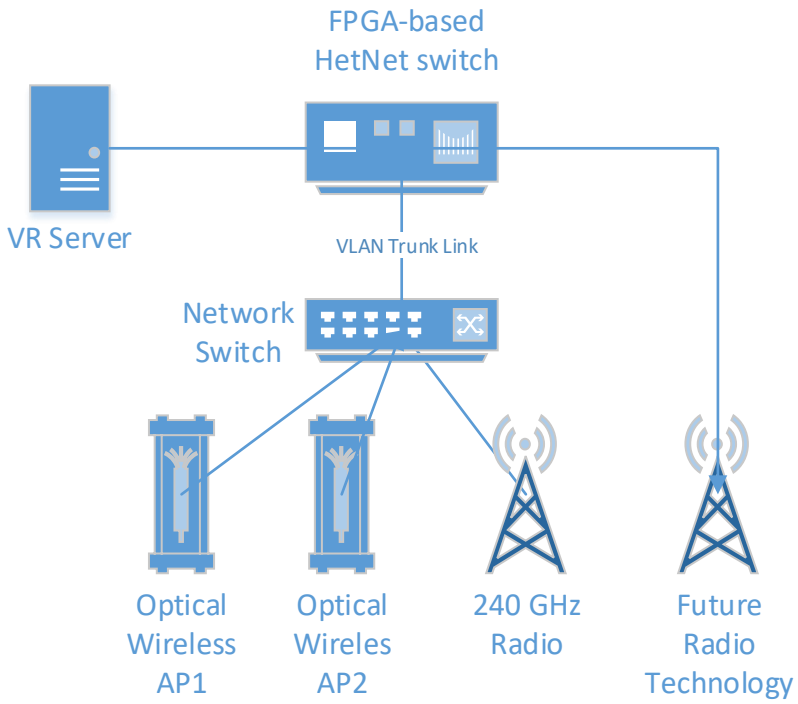

Figure 14: Integration of FPGA-based HetNet Switch (with Layer2.5 implementation) with a typical network switch to enable more physical network interfaces

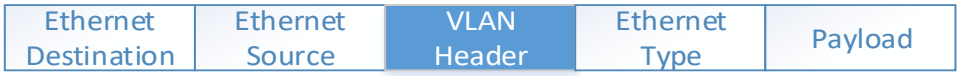

Figure 15: Ethernet frame with extra VLAN header

6 Conclusion

Currently, only the Fiber Wireless Fiber solution has exceeded the Tbit/s target with a promising potential data rate increase. This is a laboratory solution and substantial efforts must be made to reach a pre-industrial stage. The next step would be focuses on improving compactness, latency and cost.
The other technical solutions (Optical Wireless Communication and radio) and Heterogeneous Network system have the possibility of achieving this objective by using links parallelization management.

The terahertz enables new B2C/B2B applications including new security solutions, mobile health, medical services (eg. cancer detection) and intra-device communications. Additionally, the THz and the optic band can be deployed in short-, mid-, and long- range applications and services including for example Internet of nano things (IoNT), long range multi-gigabit links etc.

There are still several challenges to be addressed for Tbit/s communications:

- Identifying the most relevant B2B/B2C services requiring terabit throughputs.
- Developing an end-to-end system and network on chips that operate in the THz or Optic band, thereby enabling different range applications with throughputs up to Tbit/s.
- Implementation: The main difficulties related to the implementation and operation of Tbit/s technology is that they require a new merging heterogeneous technologies that, at the moment, are still under specification. The costs for development of these technologies require further investigation.
- The THz and the Optic band will also suffer from the similar limitations as mmWave bands in 5G: limited coverage and sensitivity to blockage. RF and/or optical localization can be implemented to ensure communication alignment into a Line-of-Sight (LoS) scenarios.

Even the THz and Optic bands are are the main enabler for vast majority of 6G applications, e.g. the ones that require extremely high throughputs, it is also important that the components operating in these high frequency bands can be available at a reasonable cost and with acceptable power consumption.

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