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Abstract

In this deliverable, the Proof of Concept (PoC) for the sub-terahertz radio, multi-gigabit modem and video compression system is presented. The radio system works in the 240 GHz band and is developed in the IHP's SiGe BiCMOS technology. A separate transmitter and receiver with on-chip antennas were designed and produced. Further, transmitter and received, working in the same 240 GHz band and having 4 on-chip antennas configured as uniform linear array, capable of beam steering were also designed and produced. These chips are intended to be used as standalone, or in combination of multiple chips, in order to create a larger antenna array. The baseband processor, i.e. the multi-gigabit modem, was developed and written in MATLAB. It has the possibility to be used in a hardware in the loop simulation, where real hardware would be used for data transmission. At the end, B<>COM has developed a video compression/decompression system and implemented it on a FPGA board. This system is capable of different compression rates while at the same time offering low latency, needed for VR applications.

Keyword list

Wireless transmission, terahertz, multi-gigabit, terabit, antenna array, beam steering, video compression/decompression

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List of Acronyms

ADC	Analog to Digital Converter
A/D	Analog to Digital
AFE	Analog Front End
AWGN	Additive White Gaussian Noise
AWGN	Additive white Gaussian noise
BER	Bit Error Rate
CFO	Carrier Frequency Offset
CIR	Channel Impulse Response
CP	Cyclic Prefix
D/A	Digital to Analog
DAC	Digital-to-Analog Converter
dB	Decibel
dc-OCL	Direct current cancellation loop
DFT	Discrete Fourier Transform
DVB	Digital Video Broadcasting
EIRP	Effective Isotropic Radiated Power
ETH	Ethernet
FEC	Forward Error Code
FFT	Fast Fourier Transform
FIR	Finite Impulse Response
FPGA	Field Programmable Gate Array
FSPL	Free space path loss
Gbps	Giga bits per second
GND	Ground
HD	High definition
HMD	Head Mounted Display
HSPA	High Speed Packet Access
IFFT	Inverse Fast Fourier Transform
ISI	Inter Symbol Interference
LDPC	Low Density Parity Check
LO	Local Oscillator
LOS	Line Of Sight
MAC	Medium Access Control

MCS	Modulation and Coding Scheme
NLOS	Non Line Of Sight
OFDM	Orthogonal Frequency Division Multiplex
P/S	Parallel to Serial
PA	Power Amplifier
PAPR	Peak-to-Average Power Ratio
PCB	Printed Circuit Board
PHY	Physical layer
PoC	Proof of Concept
PRBS	Pseudo-Random Binary Sequence
QAM	quadrature amplitude modulation
QPSK	quadrature phase shift keying
QSFP	quad small form factor pluggable
RF	Radio Frequency
RLS	Recursive least squares
RMS	Root Mean Square
RRC	Root rised cosine
SC	Single Carrier
SFP	small form factor pluggable
SNR	Signal to Noise Ratio
TM2	Top metal 2
UHD	Ultra high definition
ULA	Uniform linear array
UPA	Uniform planar array
VC	Video Converter
VGA	Variable Gain Amplifier
VR	Virtual Reality
WORTECS	Wireless Optical/Radio TErabit CommunicationS

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1. Introduction

In this deliverable, the objective is to show the proof of concept (PoC) for the sub-terahertz radio, multi-gigabit modem and video compression system. This deliverable presents only the sub-terahertz radio system developed in IHP as well as the low latency video compression/decompression system.

Within the WORTECS project IHP developed a wireless transmitter and receiver chips working in the 240 GHz band. The IHP's SiGe BiCMOS technology, having f_t/f_{max} = 300/500 GHz was used [1]. The developed chips integrate an on-chip antenna for the 240 GHz band. The developed chips were further mounted on a high frequency printed circuit board (PCB) in order to produce a complete transmitter and receiver. Additionally, IHP developed a transmitter and receiver chip with a 4 × 1 antenna array. A special precautions were taken during the design of the chips, in order to be able to construct larger antenna array. The produced transmitter and receiver chips are also capable of introducing a variable phase shift on each of the 4 antennas. This enables beam steering of the antenna array. Additionally, having 4 antennas increases the antenna gain, which is extremely important, especially because of the low output power and high noise figure (NF) at these frequencies in the used semiconductor technology. In order to enable use of multiple chips, a common local oscillator (LO) distribution is carefully planned in a multi-chip antenna array configuration.

In order to transfer a high resolution, high frame rate video, huge bandwidths are needed. In a multiuser scenario, this would easily exceed throughputs of a few hundreds of gigabits, even terabits, per second. No technology for multi-terabit wireless transmission is available at the moment, neither is envisioned within the WORTECS project. Therefore, a low latency video codec was developed in order to support the low latency requirements for the virtual reality (VR) use case in the WORTECS project. This codec supports different compression rates and low latency. It was implemented on an FPGA board.

In Figure 1 the PoC technologies which are demonstrated in the WORTECS project are shown. Most of them are described in [2]. In this deliverable only the 240 GHz radio and the video codec PoC would be described. They are marked with the red circles in Figure 1.

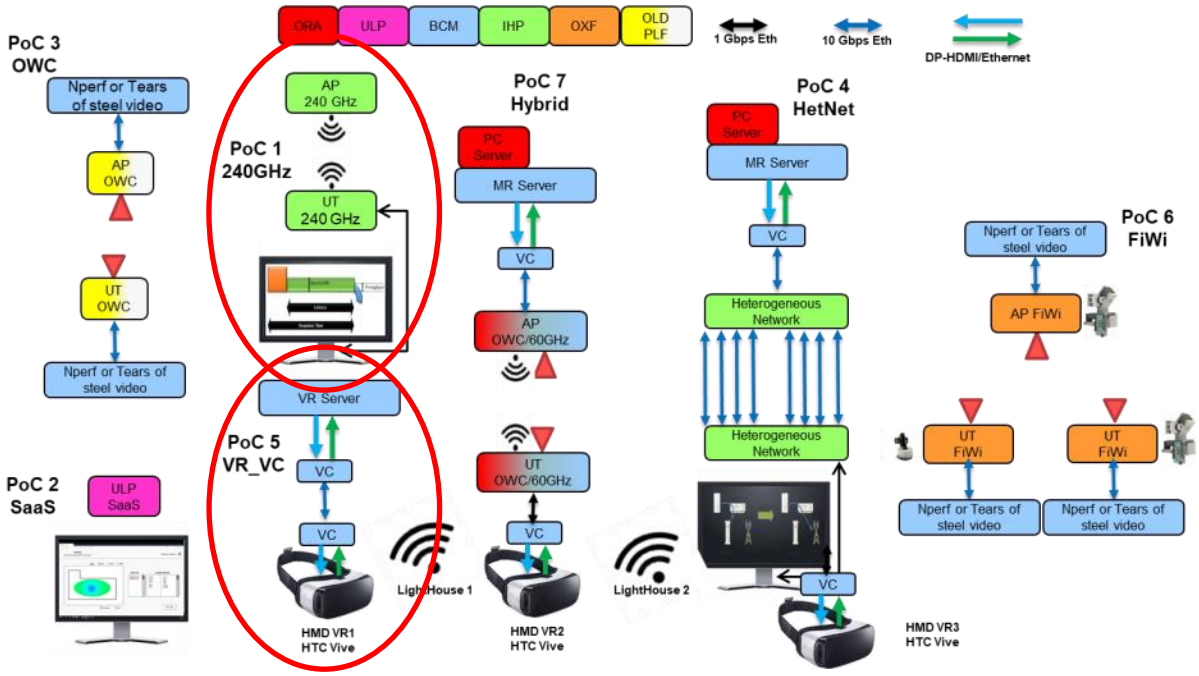


Figure 1 - WORTECS PoC technologies

2. 240 GHz radio transmitter and receiver

2.1 240 GHz IQ carrier generation

To generate the carrier signal on-chip, as shown in Figure 4 and Figure 7, a multiplier-by-8 chain is implemented. The single-ended input (LOin) cantered at 30 GHz drives an edge coupled spiral Marchand balun. A single stage multiplier-by-4 stage is followed by two stage amplifier in order to filter the quadrupler output and drives the Gilbert cell based multiplier by 2. The output of the multiplier is then amplified by 3-stage amplifier. The LO multiplier-by-8 chain achieves 55 GHz of bandwidth with 1.5 dBm output power. The differential output of the LO chain drives a differential Branchline coupler with a measured loss of 2 dB. The quadrature differential output drives then the IQ up-/down-conversion mixers. The IQ signals are generated by a differential planar edge coupled Branchline coupler. The coupler is implemented in the top most metal (TM2) with the ground plane at M3. The dimensions of the Branchline coupler was optimized after electromagnetic (EM) simulations to accommodate for the effects rising from the cross overs of the differential signals and the via connections. The simulation results shows a phase error of 3 degrees from 200 to 265 GHz and 5 degrees from 200 to 280 and gain imbalance of 1 dB from 210 to 285 GHz. In order to quantify the insertion and return loss performance parameters of the coupler, the test structure shown in Figure 1 was manufactured and measured. The planar Marchand balun is used to allow for on-wafer single ended measurements. Also the back-to-back test structure of the Marchand balun shown in Figure 2 was manufactured and measured recording a minimum loss of 1.5 dB with 1dB roll off from 200 to 260 GHz. Accordingly the Branchline coupler has a loss of only 3 dB and covers the whole J-band.

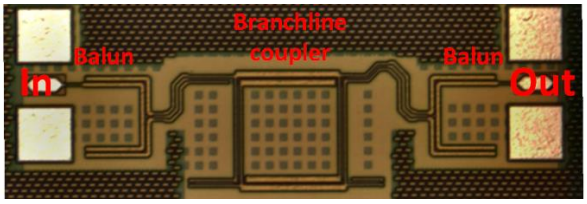


Figure 2 - Branchline coupler test structure die photo

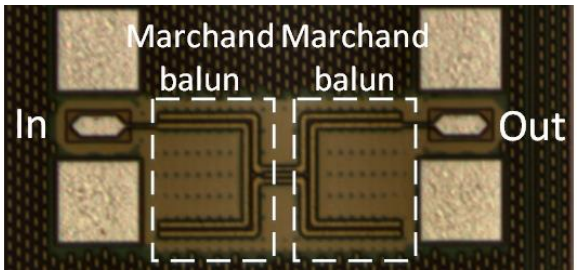


Figure 3 - Marchand balun test structure die photo

2.2 240 GHz transmitter

Direct conversion IQ transmitter is implemented as shown in Figure 3. The LO carrier is generated with a multiplier-by-8 LO chain described in the previous section. The LO chain then drives the IQ up-conversion mixers. The mixers outputs are combined and amplified with an integrated power amplifier to be radiated through the on-chip antenna. The transmitter IQ differential inputs are first buffered by a resistively loaded common-emitter input driver stage. The input is matched to 100 ohm impedance with on chip resistors, with the common node, biased internally with a resistive potential divider. In order to extend the bandwidth of the transmitter and compensate for the bandwidth limitation of the input bond wires, peaking inductors are implemented in the input stage. With such series inductive peaking the 3- dB bandwidth of the input driver is extended from 30 GHz to 60 GHz while having approximately same group delay variations. The differential broadband signal feeds a

Gilbert cell based mixer. The modulating signal is fed into the base of the switching quad while the LO signal is fed into the g_m stage. This architecture has a better conversion gain compared to the conventional Gilbert cell connection for lower LO power levels. Nevertheless, it is recommended to use this architecture at baseband input power levels near the compression point. The combining of the I and Q mixers outputs could be performed using different architectures. In some embodiments the outputs of the I-mixer and Q-mixer were directly combined at the mixers outputs and then matched to interface with the following amplification stage. This technique, although having lower losses, might have less bandwidth. At such high frequencies the output impedance of the up-converter mixer is already low, so combining the two outputs leads to higher impedance transformation ratios. On the other hand, by direct combining of the outputs the cross talk between the I-path and the Q-path might be more pronounced. This means that self-mixing at the mixer output nodes will lead to poor IQ rejection. Another approach is to match the I and Q signal each to 100 ohm impedance and then combine them with a Wilkinson power combiner. The matching of each mixer before combining has a less impedance transformation ratio, and the Wilkinson power combiner will guarantee a certain isolation between the I-path and Q-path. Hence, in this work the second approach is followed. The back-to-back Wilkinson test structure, shown in Figure 5 was measured on wafer. The minimum insertion loss of 1.5 dB was measured for the Wilkinson combiner after accounting for 1 dB loss of the balun. The flatness is better than 1.5 dB from 200 to 260 GHz. The combined modulated output signal is then amplified by a broadband 3-stage pre-driver amplifier. The pre-driver is the same amplifier used as the driver of the LO chain. The output of the pre-driver drives then the 3-stage 4-Way zero-degree power combined power amplifier. The top level simulation of the transmitter without the input bond-wire and pads, shows a 3-dB bandwidth of 46 GHz. After including the input pad, input bond wire of 550 pH and the board traces, the 3-dB bandwidth decreases to 36 GHz. The bandwidth enhancement of the inductive peaking on the top level shows that the bandwidth is enhanced by 20% from 30 to 36 GHz. The conversion gain across the LO frequency shows a 3- dB bandwidth from 210 GHz to 255 GHz. The output 1dB compression across baseband input frequency reaches a maximum output 1-dB compression point of 7.5 dBm. The die photo of the fully integrated IQ transmitter is shown in Figure 5 including the on-chip antenna.

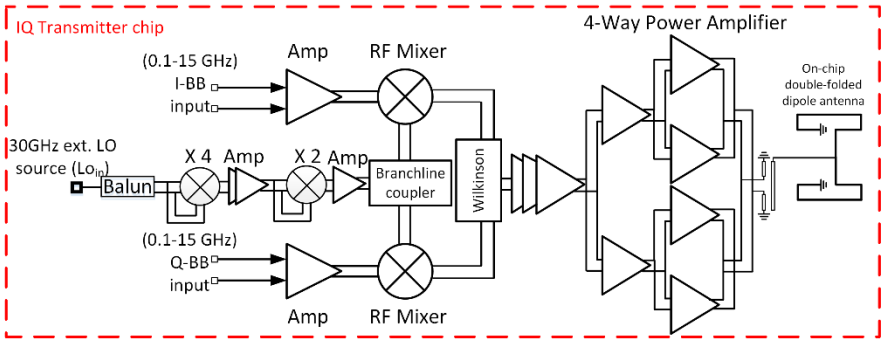


Figure 4 - IQ transmitter schematic

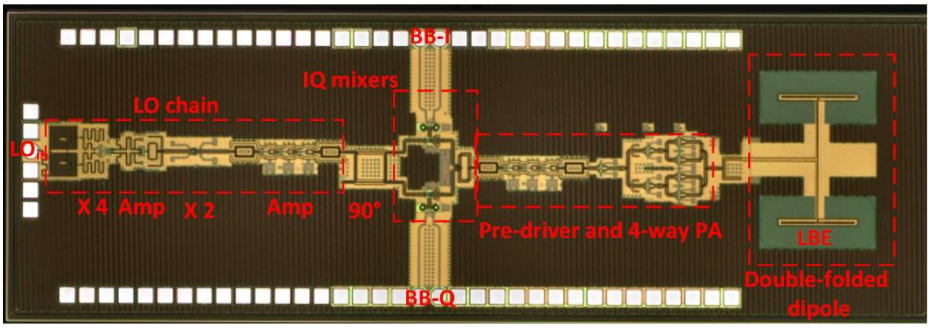


Figure 5 - IQ transmitter die photo

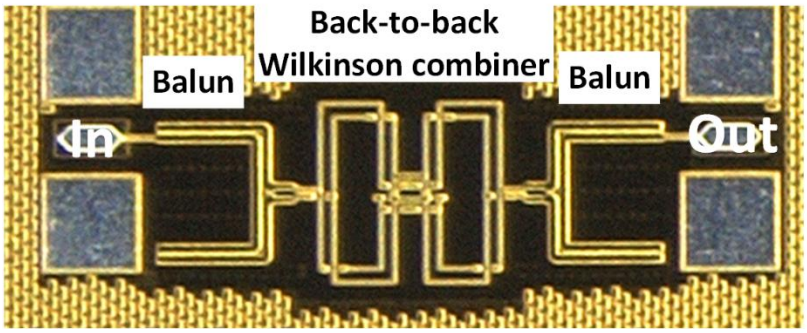


Figure 6 - Wilkinson power combiner back-to-back test structure die photo

2.3 240 GHz receiver

The receiver chip shown in Figure 7 is equipped with a single ended double folded dipole antenna feeding a three stage low noise amplifier through the edge coupled Marchand balun. The Wilkinson power splitter explained in previous section splits the output of the LNA to I-path and Q-path, feeding two switching quad mixers. The mixer is loaded with a transimpedance amplifier (TIA) to maximize the bandwidth and de-correlate the design of the mixer from the design of the TIA, therefore having more degree of freedoms to optimize for gain and bandwidth. To compensate for the losses of the Branchline coupler and power division of the LO chain, a single stage amplifier is implemented at the LO port to drive the mixer in LO saturation. The baseband chain consists of the TIA followed by two variable gain amplifiers and an output buffer. Two dc offset cancellation loops (dc-OCL) are integrated to cancel the dc-offset after the mixer and at the output of the baseband chain, keeping the differential offset below 3mV at maximum gain conditions. The first dc-OCL also serves as a cancellation loop for the residual dc-offset arising from the LO leakage in the transmitter and receiver, this is very crucial to avoid the receiver from being saturated and desensitized from high LO to RF leakage. The receiver has a simulated maximum gain of 41 dB with 20 dB of gain tuning across a 3-dB BW of 70 GHz with no bond wire. With the effect of the output bond wires equivalent to 550 pH the 3-dB bandwidth is 60 GHz. A double side band noise figure (NF) of 14 dB, without the input balun and pad. The wideband LO chain allows the receiver to operate across a 3-dB LO frequency bandwidth of 45 GHz from 210 to 255 GHz, with an LO rejection of more than 30 dBc. In the receiver layout shown in Figure 8, the LO chain was folded to reduce the chip size. The receiver consumes 0.85W from 2.5V and 3.3V supplies and 5.1mm2 of silicon area.

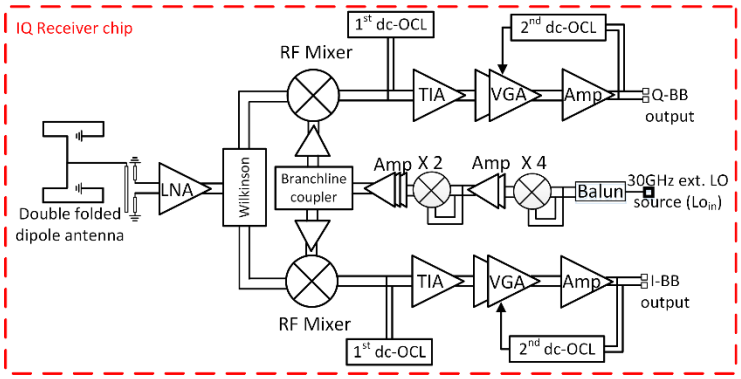


Figure 7 - IQ receiver schematic

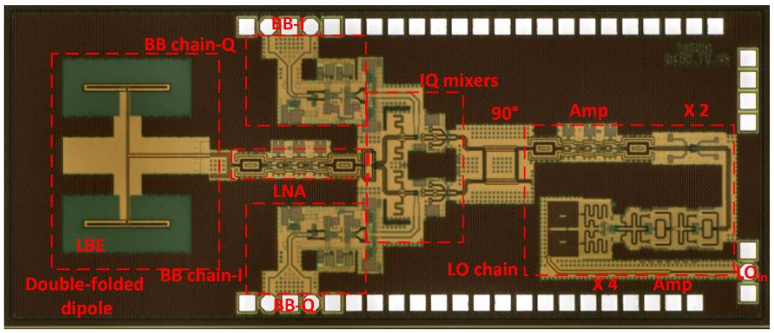


Figure 8 - IQ receive die photo

2.4 On chip folded dipole antenna

The IHP's local back side etching technology allows for high antenna efficiency by removing the high loss silicon substrate beneath the antenna radiator. The double folded-dipole antenna presented here and shown in Figure 9. The radiator is manufactured on the uppermost metal layer (TM2) with the board below the chip serving as reflector in the final implementation. The silicon substrate height is thinned to 200 um. The simulated antenna gain is 7.5 dBi with 25 degrees of beam width and a 1-dB bandwidth of 33 GHz from 225 GHz to 258 GHz, with a maximum simulated efficiency of 70%. These simulation results do not include the input pad structure. The antenna test structure shown in Fig. 18 was measured on wafer, using the metal chuck of the probe station as reflector. Then, the antenna test structure was diced and glued on the ground plane of a printed circuit board (PCB) in order to compare the performance. The measured results of 8 antennas measured on-wafer and 2 antennas measured on-PCB together with the simulated input return loss including the pad showed repetitive and reproducible antenna performance. To further improve the radiated power a 40mmx 40mm lens made of high density polyethylene with a relative permittivity of 2.32 is utilized in the final demonstrator. The lens has a planoconvex type with two refracting surfaces and a focal length of 25 mm. The gain of the lens combined with the effective gain of the on-chip antenna depends on the link distance.

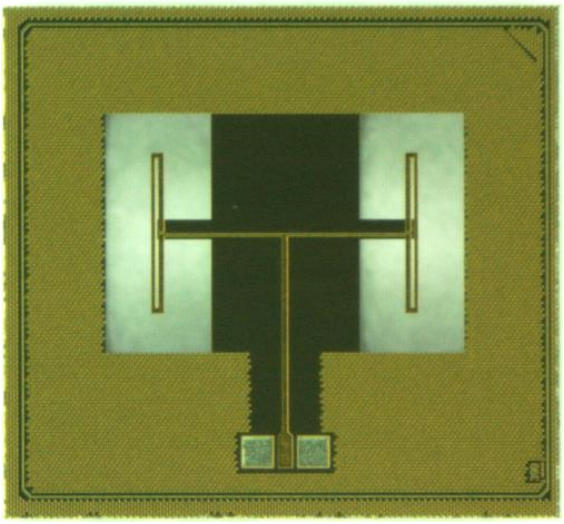


Figure 9 - On-chip antenna with LBE die photo

2.5 Antenna array

The main limitations in building transceivers working at frequencies of a few hundred gigahertz include low transmit power achievable at the transmitter and high NF of the receiver. This is especially evident in scaled technologies. Therefore, if transmitters and receivers are made in a scaled technology (CMOS, BiCMOS SiGe, etc.), where all the parts of the transceiver are integrated on a single die, it is very likely that the output power would be limited and the expected NF would be relatively high.

Taking into account high NF, low transmitter output power, as well as high free space path loss (FSPL), achieving large communication distances would be challenging in the THz band. A few approaches are available to overcome this problem. Some of them include using specific semiconductor technologies for the transmitter, which is beyond the scope of this project, since in WORTECS, IHP's SiGe technology is to be used. Another approach is to use lenses to increase the antenna gain of the transmitter and the receiver. This solution would increase the antenna gain and the communication distance respectively. The main disadvantage would be the narrow radiation pattern of transmit and receive antennas. This would make alignment of transmit and receive antennas extremely challenging, especially for the larger distances. Using these approach in a mobile scenario, like the virtual reality (VR) use case in the WORTECS project, would be practically impossible. An illustration of such a scenario is shown in Figure 10. Due to the small misalignment, the achieved signal to noise ratio would not be optimal and i.e. would be reduced. This means that the high antenna gain would be beneficial only in limited number of scenarios.

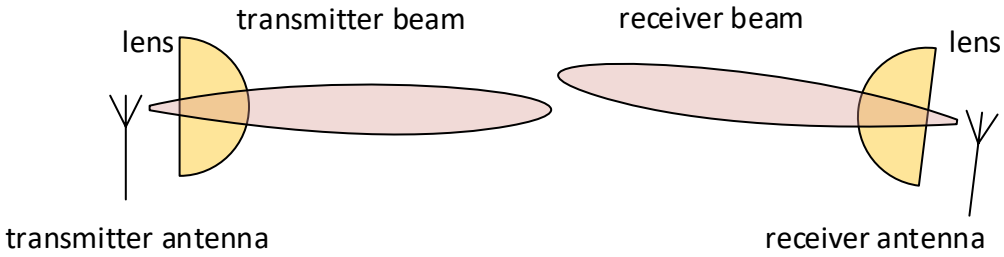


Figure 10 - Misalignment of transmitter and receiver antenna patterns (beams)

In order to overcome this, in the WORTECS project the main focus is towards building a phased antenna array system working in the 240 GHz band. Having phased antenna array system, would bring multiple advantages, which are extremely important for mobile use cases. First of all, for each antenna of the phased antenna array system, a separate power amplifier can be used. This would improve the

output power of the transmitter. Additionally, having multiple antennas, would introduce higher antenna gain. Each antenna phase can be individually changed, using a phase shifter, allowing for electronic beam steering. This would be extremely beneficial for mobile scenarios, since the antenna can be electronically steered in order to follow the users.

Within the WORTECS project, IHP has developed a transmitter and receiver chips with a uniform linear array of 4 antennas. A micrograph of the transmitter chip is shown in Figure 11.

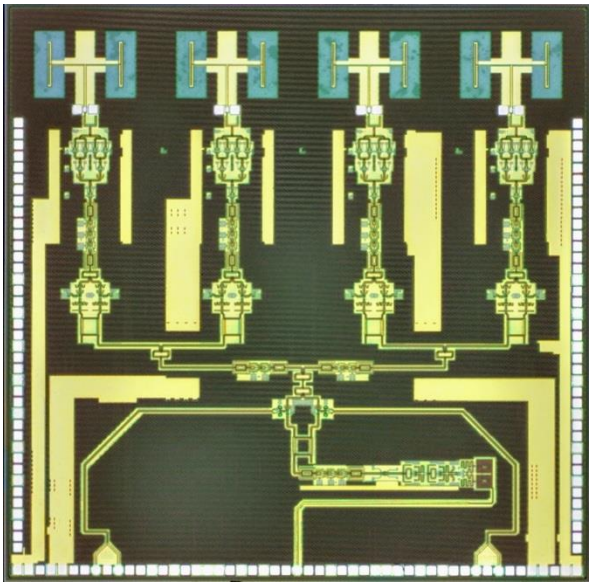


Figure 11 - Micrograph of a chip with ULA of 4 antennas working in the 240 GHz band

A simplified block diagram of the phased antenna array transmitter is given in Figure 12. Each of the phase shifters can be individually controlled, which would on the other hand steer the main beam in the required direction. The receiver has a similar configuration and 4 antennas configured in an ULA. A simplified block diagram is shown in Figure 12. Also, the phase shifters can be individually controlled in order to enable beam steering.

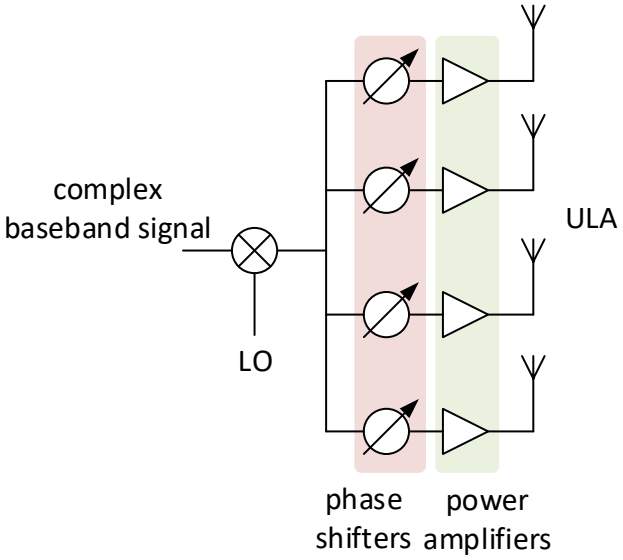


Figure 12 - Simplified block diagram of the phased antenna array transmitter

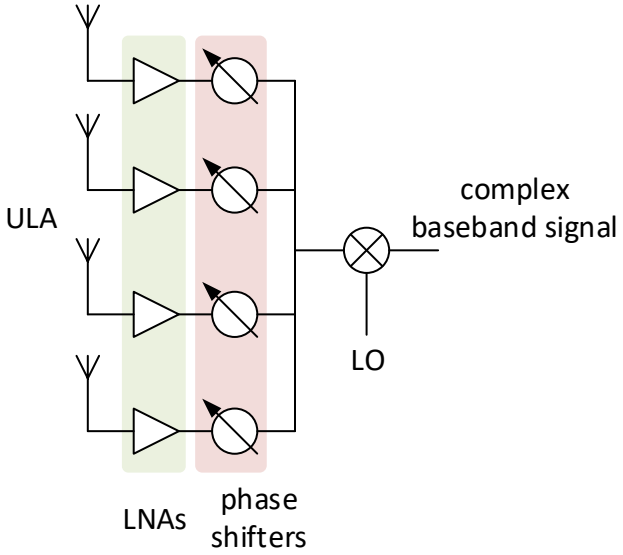


Figure 13 - Simplified block diagram of a phased array receiver working in the 240 GHz band

Having a 4 antennas would increase the antenna gain in ideal case for 6 dB. Additionally, the output power would be increased for 6 dB with respect to a single antenna system. Finally, the equivalent isotopically radiated power (EIRP) would be 12 dB better compared to a single antenna system. This would introduce improvement of 24 dB in the overall link budget if both 4 antenna transmitter and receiver would be used. Nevertheless, due to the large FSPL on these frequencies, if distances larger than a few meters are to be covered, using the 4 antenna chips developed in the IHP's SiGe BiCMOS technology, would be challenging. Therefore, within the WORTECS project, the multiple antenna chips were designed in a way which would enable combining multiple chips to form a uniform planar array (UPA). With the approach that IHP uses, ULAs with configuration of (4×N) × 1 antennas or UPA with (4×N) × 2 antennas can be built. In Figure 12 an antenna array with total of (4×2) × 2 (or 16) antennas is built.

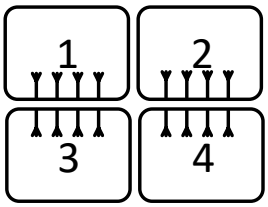


Figure 14 - UPA with 8 × 2 configuration

It can be noted that with the developed phased antenna array chips, only ULA or UPA with a maximum of two rows of antennas can be built. On one hand, this would present a limitation, but on the other hand it can be a huge advantage. Namely, having N × N (or M × N) UPA, would enable a beam steering in both direction, elevation and azimuth, and higher antenna gain, i.e. narrower beam. Nevertheless, this would lead to a complex beam search procedure, since both the transmitter and receiver should search in two dimensions which would lead to complexity of $O(N^4)$. The IHP's approach is to have narrower radiation pattern in the azimuth direction and wide radiation pattern in the elevation pattern. This means that the beam search procedure would be performed in a single plane, i.e. azimuth. The complexity of a beam search procedure would be $O(N^2)$ in this case.

In order to evaluate the proposed antenna configuration a simulation of the phased antenna array system was performed. An ideal radiation pattern of a dual folded dipole for each antenna element was used for simulation. This would not represent the realistic case, but would give a solid base for further evaluation without a loss of generality. For the simulation an ULA with 16 × 1 antennas was used. The radiation pattern in the azimuth and elevation planes are shown in Figure 15 and Figure 16 respectively. It can be noted that the width of the radiation pattern in the elevation plane is approximately 60 degrees wide, while in the azimuth plane it is not more than 5 degrees wide. Additionally, the azimuth radiation pattern is steered for 30 degrees of centre, by simply applying the appropriate phase shifts to the appropriate antenna elements.

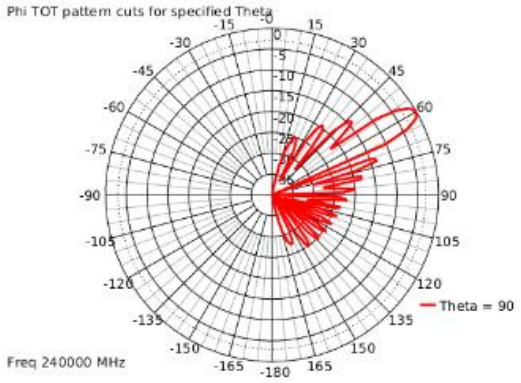


Figure 15 - Azimuth radiation patterns of the simulated antenna for the 240 GHz band

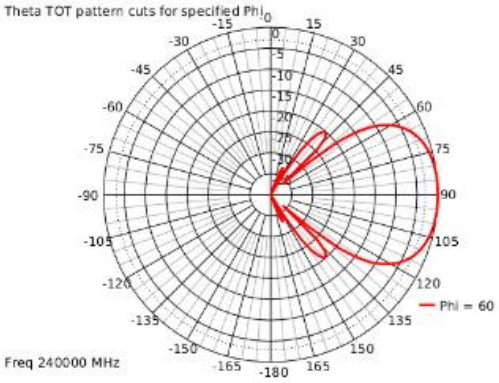


Figure 16 - Elevation radiation pattern of the simulated antenna for the 240 GHz band

In Figure 17, a 3D radiation pattern of the 16 × 1 ULA is shown. It can be seen that the pattern has a fan beam form.

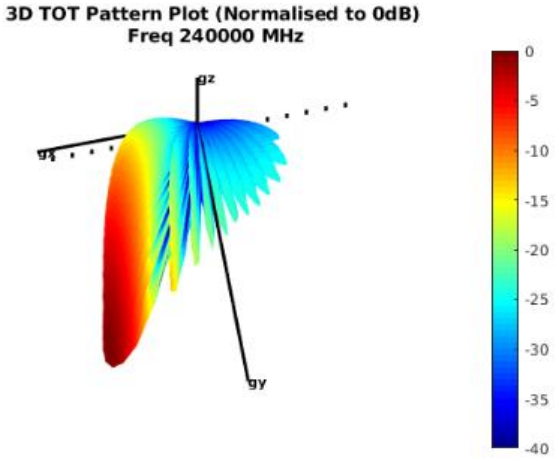


Figure 17 - 3D radiation pattern of the 16 x 1 antenna array for the 240 GHz band

3. Multi-gigabit test system

As mentioned above, the transmitter and the receiver developed at IHP have a huge bandwidth. This is of extreme advantage, since the large bandwidth enables a large channel capacity. Nevertheless, in a power-limited regime, the capacity would not linearly increase with the bandwidth. This is due to the increase of the thermal noise level with the increase of the bandwidth, while at the same time the received power is constant. The channel capacity as a function of channel bandwidth in a power-limited regime is shown in Figure 18. Since the transmit power of the transmitter is limited, the channel capacity would not linearly increase with the increase of bandwidth. Therefore, having a transmitter and receiver that support large bandwidths, it would be hardly of any benefit if the transmit power is limited and the NF is high.

Additionally, hardware implementation of multi-gigabit systems is also challenging due to the large bandwidth of the data to be processed. There are only a limited number of commercially available analog to digital (A/D) and digital to analog (D/A) converters capable of sampling bandwidths of a few tens of gigahertz.

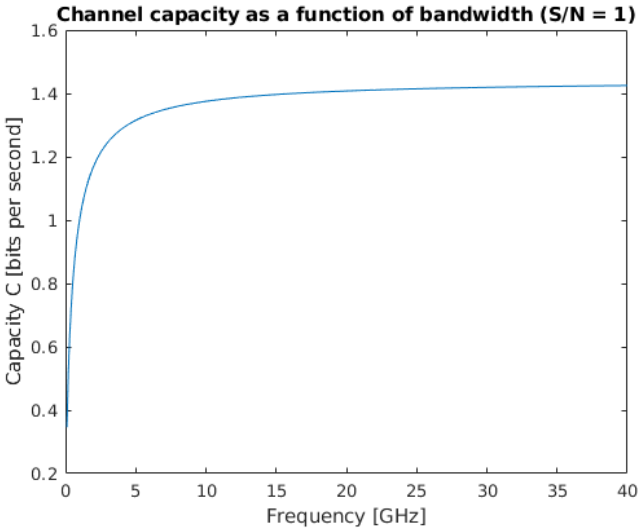


Figure 18 - Channel capacity as a function of bandwidth in a power-limited regime

Due to the mentioned reasons, having an extreme large channel bandwidths is usually not justified. Therefore, within the WORTECS project bandwidths up to 30 GHz for QPSK modulation and 25 GHz of channel bandwidth for 16 QAM modulation are considered.

In order to test the 240 GHz transmitter and receiver, a setup, as the one shown in Figure 19, was built. This setup represents a 240 GHz data transmission link. The transmitter and the receiver are spaced 0.8 meters apart. The both transmitter and the receiver have a double folded dipole on-chip antennas. Due to the low transmit power and high NF at these frequencies, additional lenses are added in order to increase the antenna gain.

The transmitter has two differential inputs for the in-phase (I) and the quadrature (Q) baseband signals to be transmitted. The baseband signals are generated using an arbitrary waveform generator, a Keysight M8195A model. The transmitted signal is received by the receiver being 80 centimetres apart. The down-converted signal is available on I and Q outputs of the receiver. This signal is sampled using an oscilloscope, in this case Keysight DSA-Z63A.

In order to test the system, IQ tools software from Keysight was used. This software is a set of scripts running in MATLAB. They are used to generate the needed waveforms for different modulations. These waveforms are sent to the AWG and the received waveforms are processed using a vector signal analyser (VSA) software from Keysight. Different modulation were tested. The transmitted data was a pseudorandom sequence. With the current setup, a data transmission throughput of 100 Gbps was achieved. The detailed results would be reported in D4.7 at the end of the project. Both the receiver and the transmitter use the same local oscillator (LO) signal which is generated using Rhode&Schwartz SMR 40 signal generator. Usually the devices should have separate LO signals, but this would not reduce the generality, since efficient algorithms for frequency offset estimation and correction exist.

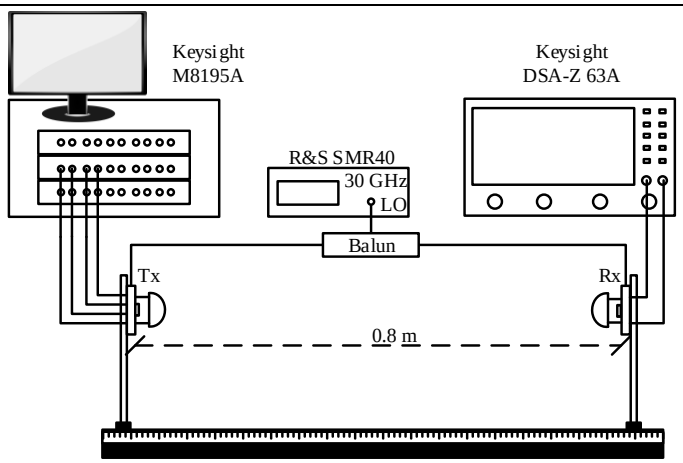


Figure 19 - Setup for testing a 240 GHz data transmission link

The photo of the setup shown in Figure 19 is shown in Figure 20.

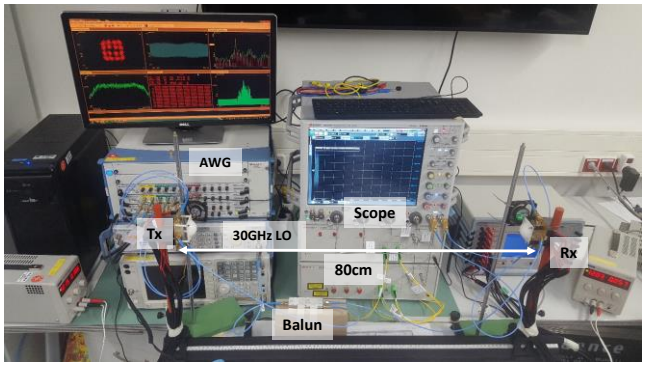
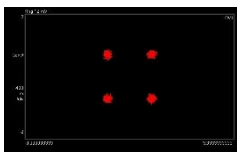
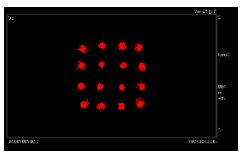


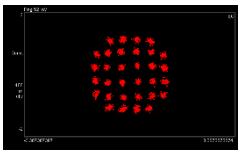
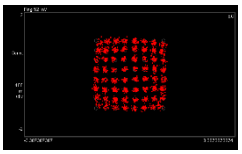
Figure 20 - Test setup for testing the 240 GHz link

The wireless link was used to transmit data with different modulations while at the same time, at the receiver, the error vector magnitude (EVM) was estimated. Having the EVM value, it would be straight forward to estimate the bit error ratio (BER) for a given modulation and symbol rate, i.e. data throughput.

Table 1 shows constellation diagrams for different modulations used on the 240 GHz system. Having a relatively low bandwidth, and relatively low data rates (the highest is 12 Gbps in this case), it is possible to use modulations up to QAM64. This is possible due to the lower channel bandwidth and, therefore, lower noise at the receiver.

Table 1 - Different constellations transferred using the 240 GHz system

Modulation	**4-QAM**	**16-QAM**
Throughput	4 Gb/s	8 Gb/s
Constellation		
Tx-Rx EVM	7.5 %	8.4 %
Modulation	**32-QAM**	**64-QAM**
Throughput	10 Gb/s	12 Gb/s

Constellation		
Tx-Rx EVM	8.5 %	8.5 %

The eye diagrams for the modulations show in Table 1 are shown in Figure 21. As can be noticed, the eye diagrams show significant opening of the eye allowing for relatively low BER. Nevertheless, in the 100 Gbps experiment, a QAM16 modulation was used. Higher order modulations are not possible in this case since the large channel bandwidths introduce high noise at the receiver.

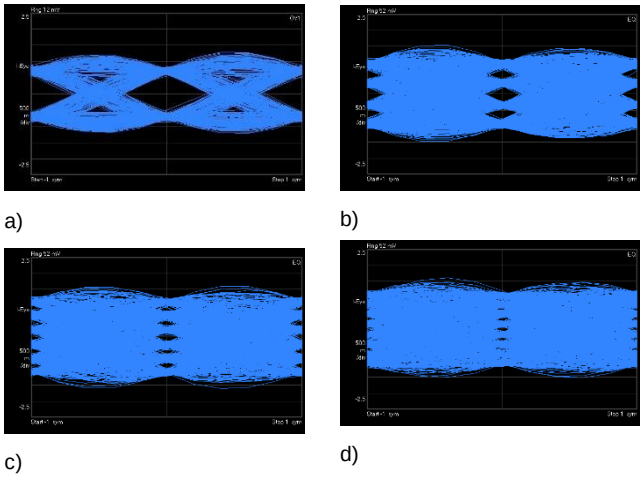
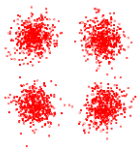
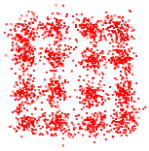


Figure 21 - Measured eye diagram of a) 4-QAM, b) 16-QAM, c) 32-QAM and d) 64-QAM.

Additionally, with the same setup were achieved data transmission rates of 80 Gbps and 110 Gbps using QPSK and 16-QAM modulations. The constellations diagrams from the symbols acquired at the receiver are shown in Table 2. As can be seen in Table 2, the corresponding error vector magnitudes (EVM) are 28% for QPSK and 20% for 16-QAM. This corresponds to bit error ratios (BER) of 2×10^{-3} and of 9.3×10^{-3} respectively. In the technical literature, the performance requirement for coded BER is typically 10-6. According to [3], the uncoded BER can be set to 10^{-2} to fulfil the requirement. This would be possible thanks to advances in the field of forward-error correction. For example, [4] presents a single-core IEEE802.11ay LDPC decoder achieving 112-Gb/s when implemented in a 16-nm FinFET technology. For QPSK, a 4-bit fixed-point implementation of that decoder with 4 iterations and a code rate of 0.875 requires Eb/N0 ≈ 5.1 dB to achieve the coded BER of 10-6 in an AWGN channel.

Table 2 - Performance limits for the tested system

Modulation	**QPSK**	**16-QAM**
Data rate	40 Gbd → 80 Gb/s	27.5 Gbd → 110 Gb/s
Const. plot		
e2e EVM	28% (-11 dB)	20% (-14 dB)

4. Baseband signal processing system

Within the WORTECS project a baseband (BB) signal processing system, i.e. baseband processor model was developed. The BB processor model was written in MATLAB. It can be used in a simulation scenario, where the channel model and the impairments of the wireless data transmission system are also modelled in MATLAB. Additionally, this BB processor model can be used in a hardware in the loop (HiL) simulation, where the data transmission is performed using a real wireless data transmission system. In this case, the developed 240 GHz system was used for data transmission.

4.1 Baseband signal processing system architecture

In Figure 22 the architecture of the developed baseband processor is shown. A few main parts are to be identified:

At the transmitter:

- Data generator
- LDPC encoder
- Preamble generator
- Up-sampler
- Root raised cosine (RRC) filter

At the receiver:

- RRC filter
- Timing extraction and synchronization
- Down-sampler
- Channel estimation (equalizer training block)
- Channel equalization (deconvolution)
- Demodulation
- LDPC decoding

The **data generator** is used to generate a random data to be transmitted. Usually, in a real system there would be a real data source (e.g. video source, audio etc.), but for a simulation or testing a real system in a HiL scenario, a random generator would be a better option.

The **low density parity check** (**LDPC**) is a forward error correction (FEC) code used to improve the BER of the system. Due to the high NF of the receiver and low transmit power of the transmitter, it is necessary to use a strong FEC code in order to achieve satisfactory BER values.

Since the main use case in the WORTECS project is a virtual reality (VR) video transmission over a 240 GHz wireless link, a LDPC code used in DVB-S2 is adopted in this BB processor [5]. The coding ratio of the used code is 2/3, but this can be changed depending on the required BER and the current scenario.

The **preamble** is used for performing timing synchronization, frequency offset estimation and correction, phase offset estimation and correction as well as channel estimation. The preamble is consisted of 2 parts. The first part of the preamble contains 10 m-sequences, being the last one inverted. The m-sequences are each 63 symbols long. The second part of the preamble uses longer m-sequences (i.e. 255, 511 or 1023 symbols long) as a training sequence for the RLS-channel-equalization at the receiver. The training-sequence is transmitted twice, first in I then in Q component. Between the first and second part of the preamble, as well as between the preamble and the payload, guard-intervals are inserted. These guard intervals should be set at least as long as the expected channel impulse response length (i.e. channel delay spread).

The **up-sampler** is needed for the used **RRC** filter. The RRC filter is used as a matched filter as well as a pulse shaping filter to minimize the inter-symbol interference (ISI). It is split between the transmitter and the receiver.

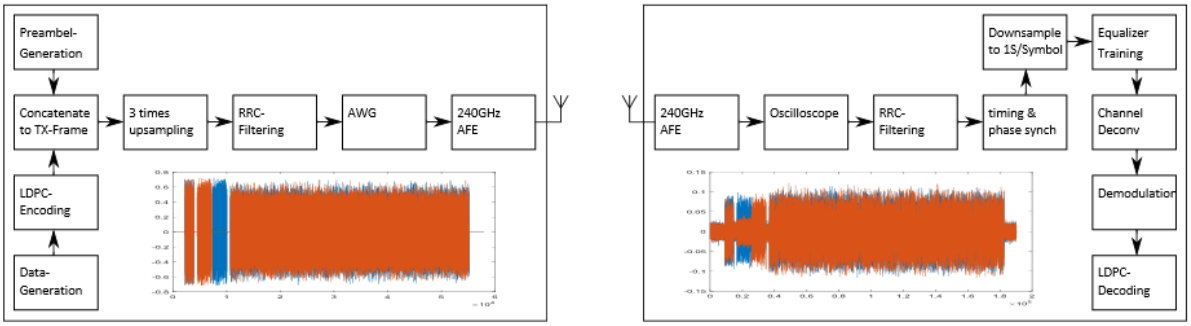


Figure 22 - Baseband processor architecture

The signal at the receiver is first filtered using the RRC filter and then **frequency synchronization** is performed. For this, the 10 short m-sequences of the preamble are used. Further, **timing synchronization** is performed by correlating the incoming preamble with a locally generated m-sequence. The acquired correlation peaks are used for timing synchronization, while, at the same time, the phase of the correlation peaks is used for **phase correction**. In this case only a single stage frequency offset estimation is performed. If a large frequency offset is expected, a two stage frequency offset estimation and correction can be implemented. Since in our case the same LO was used for the transmitter and the receiver, the frequency offset estimation and correction was not tested in the HiL scenario.

The **channel equalizer** used in this baseband processor is a linear recursive least square (RLS) equalizer [6]. The equalizer is first trained using the second part of the preamble (long m-sequence). With the trained linear RLS equalizer, a channel equalization (deconvolution) is performed. The equalization is performed for each frame. The use of the channel equalizer can be questionable in this case, since with the used system, it is very unlikely that a multipath propagation would occur. The system uses lenses which additionally increase the antenna gain. With this antenna gain, the radiation patter main lobe would be only a few degrees wide, making it impossible to have multipath propagation. Anyway, for scenarios where antenna arrays would be used, in order to facilitate shorter beam search procedures, a wide antenna radiation pattern in the elevation direction would be used. Therefore, at least ground reflection is expected.

Since the baseband signal has a large bandwidth, i.e. 15 GHz or more, usually the cables used for this signal would introduce linear distortion, i.e. attenuation, especially in the higher frequencies. This can be corrected also with the channel equalizer, but this would also introduce additional noise when the higher frequencies are amplified. Therefore, the cables, or printed circuit board tracks, should be either compensated, or additional pre-distortion should be performed. This functionality is not implemented in the baseband processor developed in WORTECS.

Finally, the developed baseband processor can be deployed in three different scenarios.

1. Simulation without any hardware specific restrictions,
2. With all resampling filters integrated but without using the instruments for HiL and
3. HiL Simulation with Keysight AWG (M8195A) and oscilloscope (DSAZ634A).

Three different types of data as payload can be used:

1. a build in random packet generator,
2. a build in test-signal (sawtooth) or
3. external data

5. Video conversion and compression

5.1 Goal

To illustrate the wide bandwidth of the wireless link, a virtual reality use case is selected. For that, we need black boxes that would realize the interface between the video signals and the transceiver. Two of them will be used, one between the video server and the transceiver inputs, and one between the transceiver outputs and the HMD.

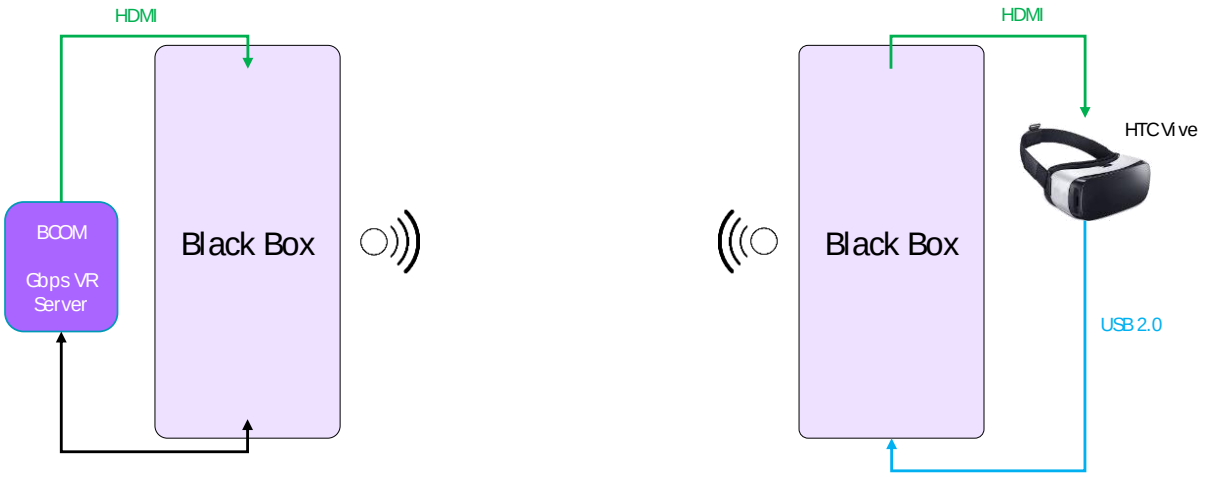


Figure 23 - Video converter goal presentation

5.2 Specifications

First of all, it should support the specific video format of virtual reality, wider and faster than classical format. The HTC Vive head mounted display (HMD) has a video resolution of 2160x1200@90Hz ≅ 5,7Gbps. It is quite different from HD or UHD broadcast resolution, and could make it difficult to find device that support this standard. The required connector is the HDMI.

Furthermore, the box should be full duplex. In one way, there is the video data flow, and in the other one, there is the localization information from the HMD. It is a low data rate (few Mbps) but mandatory. The required connector is the USB-2.0.

Regarding the transceiver interface, we need a common interface, well defined and with large capacity. The 10G Eth over SFP+ was selected because:

- It is a well-known and available standard that could be found on many hardware solutions
- Test and validation pattern can be generated with a PC with a SFP+ extension card onto PCIe
- It support both copper (well suited for laboratory test) and optical link (easier integration)

Additionally, the converter should have a low processing latency. The main reason of this is that VR is a closed loop system. When the user move, its localization is updated, sent to the computer, which creates the new corresponding picture, sends it to the HMD and displays it in front of the user eyes. To prevent motion sickness of the user, all these operations should be performed in less than 20ms. If we look closer to the system, the VR set up already consume approximately 15ms, that means additional components should not increase the overall latency for more than 5ms. If we consider that the signals would be processed from a pair of converters twice (a first one in uplink, and a second one in downlink), one pair should have a maximum latency of 2ms.

Finally, for an easier integration and to avoid components damage, a packaged solution should be considered.

In the first approach, we reviewed the existing products already available on the market. In all the reviewed products we found that none of them was achieving all the necessary requirements. Some of them were using a standard SFP+ connector, but with a proprietary protocol, perfect for some point to

point link between to converters. Nevertheless, implementing their protocol in the WORTECS transceiver was not possible. They were not compatible with the video format (their targeted market HD or UHD), or they used video compression to reduce the Ethernet throughput with a resulting processing latency being too high (> 10 ms).

5.3 Hardware selection

Having in mind the high data rate and the large number of interfaces needed, a decision to use an FPGA based platform was made.

An Arria® 10 GX FPGA Development Kit from Intel was chosen. It natively supports SFP+ and QSFP+ interfaces. Additionally, an HDMI acquisition daughter board from Bitec was added on the high speed FMC port.

Regarding the USB connection, a solution from Barco that allow the USB to 1 Gbit Eth conversion in less than 190µs, is used.

If the wireless link capacity is smaller than 5.7 Gbps, a low latency compression codec from IntoPIX is used. The IP allows a compression ratio from 1 to 6.8, being the latency same regardless of the used compression ratio. It is less than 200µs for the encoder, and less than 100µs for the decoder.

5.4 Overview

Figure 24 shows the various function implemented in the two FPGA board used.

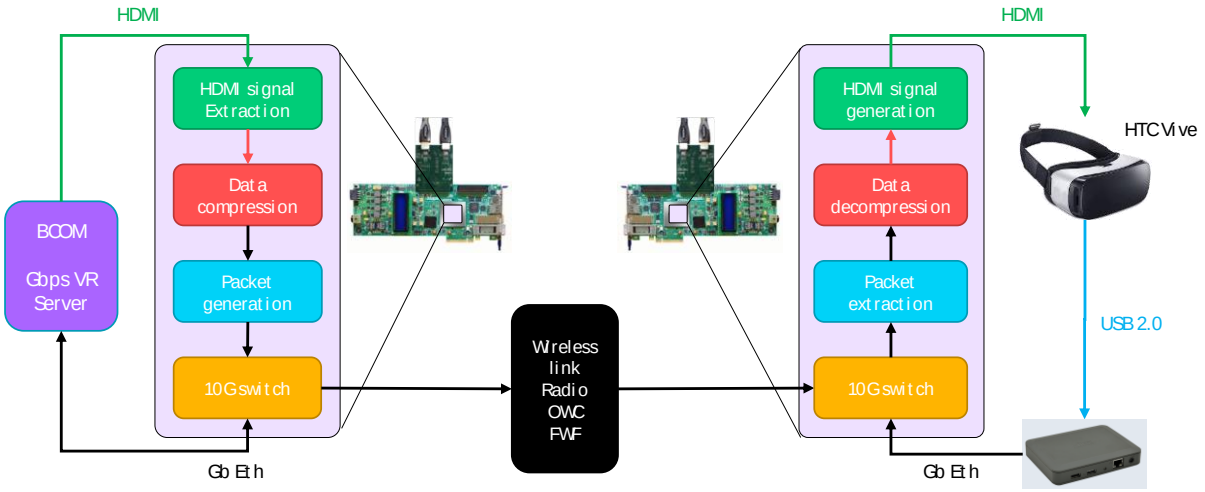


Figure 24 – System and function overview

On the computer side, the video signal is brought on the HDMI acquisition board, and it is extracted by the FPGA. The resulting video signal is compressed using low latency codec from IntoPIX, and the resulting data flow is formatted with respect to the low latency 10G Eth protocol. An additional internal 10G switch is developed to allow data circulation to and from the SFP+ external connector.

On the HMD side, data coming from the SFP+ connectors are forwarded by the internal switch to the packet extraction module. The IP address is removed and only the video payload is kept. The resulting data are uncompressed by the low latency decoder and the video signal reconstructed by the HDMI IP. This signal is further made available on the HDMI connector.

The HMD localization data, is available on a 1G Eth interface through the Barco component. It is further fed the internal 10G switch and sent out of the FPGA board through the SFP+ interface.

Once received on the other side, the ETH signal is directly forwarded to the computer through the 10G switch.

5.5 Integrated features

Two IP are integrated in the FPGA design. The first one from IntoPix for low latency compression and decompression, and the second one from Intel for the 10G Eth standard support. Additional functions are developed to make these IP integration and utilization easier.

5.6 Developed features

To improve robustness, additional functions have been implemented. First, on the HMD side, we need to generate the video clock. Usually, it comes from the video server, in phase with the video data flow. Since the emitter and receiver are split, this clock needs to be regenerated. The packet structure of the Ethernet protocol makes it difficult to recover a continuous clock and some closed loop tracking system is required to support non constant transmission latency and eventually packet loss. Regarding this last point, a detector is replacing missed packets with some padding in order to keep the system consistent and enable easier clock recovery.

An LCD is also available in order to facilitate easier debugging. It shows information about the optical power received from the optical SFP+ transceiver and shows if optical signal is present on the LC-LC optical jumper. Additionally, the board temperature is shown. Information about the peak and average received bitrate is shown, to enable easy debugging of the system throughput. Finally, it gives an information about the packet loss.

5.7 Packaged solution

In order to protect the equipment, a package is designed and manufactured. As a good trade-off between robustness and weight, 2U plastic rack was selected. All electronic equipment are integrated inside the rack and all connectors are mounted on the front panel:

- Power connector that provide +12V a +5V
- HDMI input or output depending on the used rack
- SFP+ optical jumper
- Ethernet RJ45 output for the computer side converter

Two fans ensure a continuous air flow over the components to maintain a low temperature in the rack.

Figure 25 shows the different components and the connectors on the front panel.

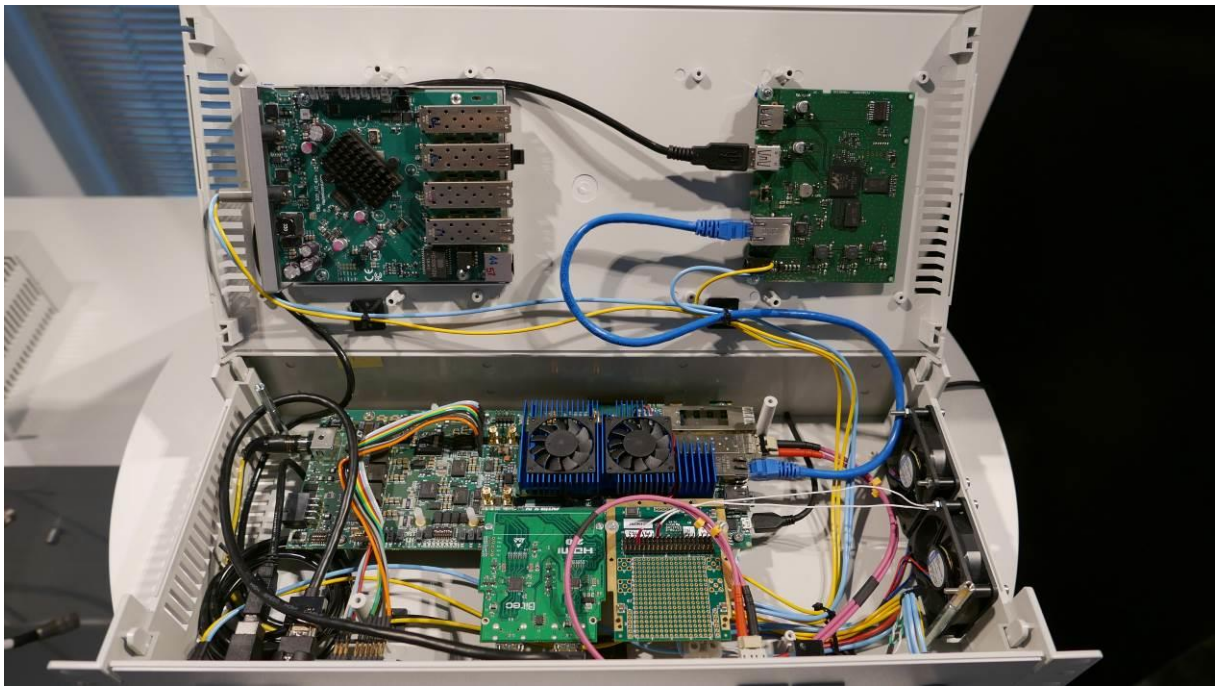


Figure 25 - Electronic components integration in a 2U rack

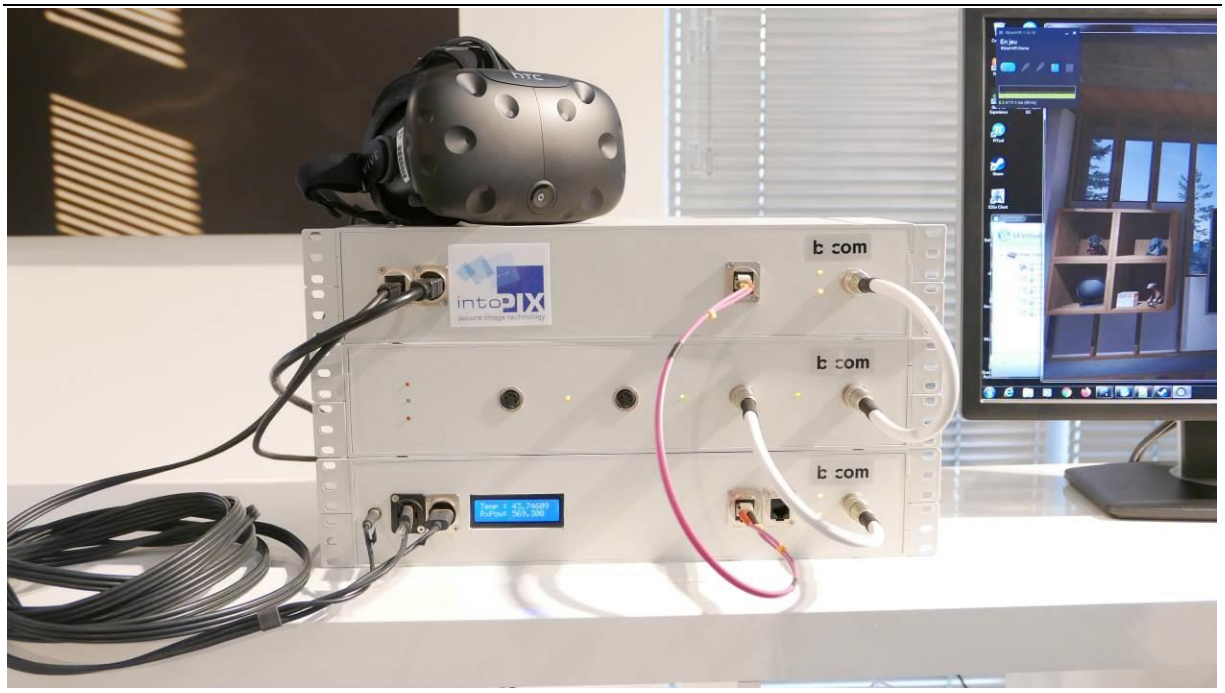


Figure 26 – Full set up with video encoder (top), power supply (middle) and video decoder (bottom)

5.8 User test acceptance

Finally, to check the compressed picture quality and the added latency effect, a user test acceptance campaign was organized. The first session was used to track reference system latency effect, while the second session was used to track both video converter latency and high compression ratio effects.

The conclusion of these tests was that neither latency nor picture quality degradation was detected.

6. References

[1] B. Heinemann and H. Rücker, "SiGe BiCMOS technology for mm-wave systems,," in *2012 International SoC Design Conference (ISOCC)*, Jeju Island, 2012.

[2] WORTECS, "D4.5 Deliverable".

[3] W. Liu, T. Wei, Y. Huang, C. Chan and S. Jou, "All-Digital Synchronization for SC/OFDM Mode of IEEE 802.15.3c and IEEE 802.11ad," *IEEE Transactions on Circuits and Systems,* vol. 62, no. 2, pp. 545-553, 2015.

[4] M. Li, V. Derudder, C. Desset, A. Dewilde, A. Bourdoux and Y. Huang, "A 100 Gbps LDPC Decoder for the IEEE 802.11ay Standard," in *IEEE 10th International Symposium on Turbo Codes & Iterative Information Processing (ISTC)*, Hong Kong, 2018.

[5] E. T. S. Institute, "ETSI Standard EN 302 307 V1.1.1: Digital Video Broadcasting (DVB); Second generation framing structure, channel coding and modulation systems for Broadcasting, Interactive Services, News Gathering and other broadband satellite applications (DVB-S2)," Valbonne, France, 2005.

[6] B. Farhang-Boroujeny, Adaptive Filters: Theory and Applications, Chichester, England: John Wiley & Sons, 1998.